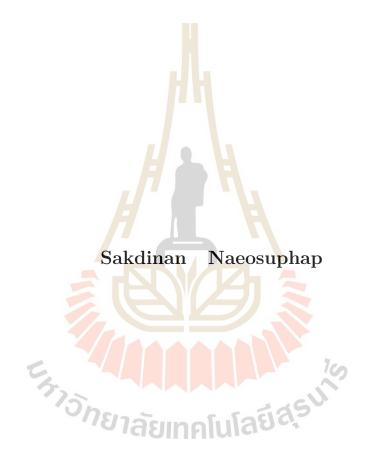
## STUDY OF HIGH RESISTIVITY SILICON WAFERS FOR ALICE PIXEL DETECTORS



A Thesis Submitted in Partial Fulfillment of the Requirements for the Degree of Master of Science in Physics Suranaree University of Technology

Academic Year 2019

การศึกษาแผ่นซิลิกอนเวเฟอร์สภาพต้านทานสูง สำหรับเครื่องตรวจจับจุดภาพของอลิซ



วิทยานิพนธ์นี้เป็นส่วนหนึ่งของการศึกษาตามหลักสูตรปริญญาวิทยาศาสตรมหาบัณฑิต สาขาวิชาฟิสิกส์ มหาวิทยาลัยเทคโนโลยีสุรนารี ปีการศึกษา 2562

## STUDY OF HIGH RESISTIVITY SILICON WAFERS FOR ALICE PIXEL DETECTOR

Suranaree University of Technology has approved this thesis submitted in partial fulfillment of the requirements for a Master's Degree.

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ALICE (A Large Ion Collision Experiments) ซึ่งเป็นหนึ่งในสถานีวัดของ CERN (the European Organization for Nuclear Research) โดยในระหว่างปี ค.ศ. 2012-2018 ได้พัฒนาและ ้ปรับปรุงหัววัครุ่นใหม่และทำการทดสอบ<mark>แล</mark>ะติดตั้งในปี ค.ศ. 2019-2020 โดยในการปรับปรุง ้ครั้งนี้มีเป้าหมายเพื่อทำให้สามารถศึกษ<mark>าสถา</mark>นะ ควาร์ก-กลูออน พาสม่า (Quark Gluon plasma state) โดยหนึ่งในส่วนสำคัญที่ทำการปรับปรุงครั้งนี้คือส่วน Inner Tracking Systems (ITS) ซึ่ง เป็นส่วนที่อยู่ใกล้สุดจากจุดการชนกันของอนุภา<mark>ก</mark> โดยทำหน้าที่เป็นตัวตรวจจับ (sensing) อนุภาก ต่าง ๆ ที่เกิดขึ้นหลังการชนกันของอ<mark>นุภา</mark>คหลัก ร<mark>ะบ</mark>บ ITS นี้เป็นส่วนที่อยู่ใกล้กับจุดที่เกิดการชน กันของอนุภาคหลักมากที่สุด และชิ้นส่วนที่สำคัญของระบบ ITS คือ ซิลิกอนเซนเซอร์ที่เรียกว่า ALICE Pixel Detector (ALPIDE) โดยALPIDE ได้ใช้เทคโนโลยี Monolithic Active Pixel Sensors (MAPS) ซึ่งเป็นเทคโนโลยีที่รวมตัวเซ็นเซอร์และวงจรลอจิกเข้าไว้ด้วยกัน ส่งผลให้ได้ เซ็นเซอร์มีความเร็วในการอ่านข้อมูลที่มากขึ้น บางขึ้น และใช้พลังงานน้อยลงทำให้สามารถเพิ่ม ประสิทธิภาพในการติดตามเส้นทางของอนุภาค (particle tracking)ได้ด้วย ดังนั้นเพื่อสร้าง APIDE จึงต้องใช้แผ่นซิลิกอน (silicon wafer) ชนิดบางเป็นพิเศษและต้องมีความหนาของชั้น epitaxial layer เพียง 25 ไมโครเมตร<mark> อย่างไรก็ตามเมื่อเซนเชอร์มีความ</mark>หนาน้อยลงจะส่งผลให้เกิดปัญหา เรื่องความทนทานเนื่องจากเซนเซอร์ต้องทำงานในจุดที่ใกล้การชนของอนุภากที่มีการปลดปล่อย รังสีปริมาณที่สูงมาก เซนเซอร์จึงต้องมีความทนทานต่อรังสี (radiation hardness) นอกจากนี้ โครงสร้างของ MAPS มักมีผลกระทบจากรังสีมากกว่าเซ็นเซอร์แบบเก่าอีกด้วย ดังนั้นการ ตรวจสอบแผ่นซิลิกอนเวเฟอร์ซึ่งเป็นวัสดุตั้งต้นในการสร้าง ALPIDE และการศึกษาผลกระทบ ของรังสีต่อเซ็นเซอร์จึงมีความจำเป็นอย่างมากต่อการออกแบบและทดสอบเซ็นเซอร์ที่สามารถ ทนรังสีได้ในปริมาณดังกล่าวและเนื่องจากโดยพื้นฐานแล้วเซ็นเซอร์มีโครงแบบเดียวกับไดโอด ด้วยเหตุนี้การศึกษาส่วนใหญ่จึงสามารถใช้ไดโอดในการศึกษาคุณสมบัติเบื้องต้นของเซ็นเซอร์ได้

ดังนั้นในงานวิจัยนี้ในส่วนแรกได้ทำตรวจสอบคุณสมบัติทางไฟฟ้าและความหนาของ ชั้น epitaxial ของแผ่นซิลิกอนสภาพต้านทานสูงด้วยวิธีการ Four-Point Probes (4PP) Spreading Resistance Profiling (SRP) และ Scanning Electron Microscope (SEM) เพื่อเป็นข้อมูลสำหรับใช้ สร้าง ALPIDE ในส่วนที่สองได้ทำการศึกษาผลกระทบของรังสีต่อไดโอดที่มีโครงสร้างที่ แตกต่างกันเพื่อหาบัจจัยที่ส่งผลต่อการเปลี่ยนแปลงของเซ็นเซอร์เมื่อได้รับรังสีที่ปริมาณต่างกัน โดยได้ทำการสร้างไดโอดขึ้นมาสองแบบและนำไปฉายด้วยอิเล็กตรอนและรังสีแกมมา จากนั้น ทำการวัดคุณสมบัติทางไฟฟ้าที่เปลี่ยนไปหลังการฉายรังสีด้วยวิธีการกระแส-ความต่างศักย์ (I-V) และวิธีการความจุ-ความต่างศักย์ (C-V) ซึ่งด้วยวิธีการดังกล่าวทำให้สามารถทราบค่ากระแสรั่ว (Leakage current) ความจุไฟฟ้า (Capacitance) ความเข้มสารเจือยังผล (Effective doping concentration) และค่าสัมประสิทธิ์ความเสียหายจากรังสี (radiation damage coefficient) ในส่วนที่ สามได้ศึกษาผลกระทบต่อรังสีของซิลิกอนสภาพด้านทานสูงและซิลิกอนไดอ็อกไซด์ (SiO<sub>2</sub>) ซึ่ง วัสดุทั้งสองชนิดเป็นวัสดุหลักภายในเซ็นเซอร์ โดยได้นำวัสดุดังกล่าวไปฉายด้วยรังสีเช่นเดียวกับ ส่วนที่สองและนำมาตรวจสอบด้วยวิธีการ X-Ray Diffraction (XRD) และ Atomic Force Microscopy (AFM) เพื่อศึกษาโครงสร้างและพื้นผิวที่เปลี่ยนแปลงหลังการฉายรังสี



สาขาวิชาฟิสิกส์ ปีการศึกษา 2562

ลายมือชื่อนักศึกษาสิ่	กลีนันท์ เมนอสู่อาณ
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SAKDINAN NAEOSUPHAP : STUDY OF HIGH RESISTIVITY SILICON WAFERS FOR ALICE PIXEL DETECTORS THESIS ADVISOR : ASST. PROF. CHINORAT KOBDAJ, Ph.D. 97 PP.

### HIGH RESISTIVITY SILICON WAFER/DIODE CHARACTERIZATION/A LARGE ION COLLIDER EXPERIMENT/MONOLITHIC ACTIVE PIXEL SENSOR/ALICE PIXEL DETECTOR SENSOR/ ELECTRON RADIATION/ GAMMA RADIATION/C-V CHARACTERIZATION/XRD

Suranaree University of Technology (SUT) collaborates with Thai Micro Electronic Center (TMEC), and A Large Ion Collider Experiment (ALICE) to collaborate to develop a new silicon sensor for the Inner Tracking System (ITS) for particle tracking in high energy physics. In this project, the ALICE new sensor is requested to be 50 microns thick, the reason is to reduce its material budget that relates directly to the thickness of the sensor. Consequently, there use ultrathin silicon wafers with 25 microns thickness and high resistivity. Before using the wafers, the doping concentration and epitaxial layer depth are measured using Spreading Resistance Profiling (SRP) and Scanning Electron Microscope (SEM). After wafer characterization, our results show that it can obtain high resistivity wafers up to 1.6 k $\Omega$  cm that has an epitaxial layer of 25 microns to be starting materials for ALICE PIxel DEtector (ALPIDE) sensor. In addition, one of the design goals for ALPIDE sensor is to operate inside a high radiation environment above 2700 krad before deterioration. Since these sensors will be required to operate inside very harsh radiation environments, all sensors used must be able to tolerate high levels of radiation. Therefore, materials found inside silicon detectors, such as  $SiO_2$  and Si, must be carefully studied for their irradiation effects.

To study and optimization the electrical properties changes of sensor before and after irradiation, we created the simplest semiconductor detector as a reversebiased diode called perimeter diode  $(D_P)$  and area diode  $(D_A)$  from a standard wafer. This study focuses on CMOS diodes in two different designs. Besides, we studied the radiation effect in terms of the micro-structure on the high resistivity silicon wafer and Si/SiO<sub>2</sub> wafers.

In this work, we considered two aspects, structural and electrical changes, after irradiated with 10 MeV electron and gamma source with different adsorption doses rate. To study the electrical changes after irradiation  $D_P$  and  $D_A$  CMOS diodes were characterized by current-voltage (I-V) and capacitance-voltage (C-V) characteristics with a temperature of 300 K°. Microstructure defects and structural changes from the irradiation effect of high resistivity Si(100) and Si(100)/SiO<sub>2</sub> wafers have been characterized by X-ray Diffraction (XRD) and Atomic Force Microscopy (AFM). The I/V results show increasing in leakage currents and the C/ V results show a slightly decreasing in capacitance of  $D_P$  and  $D_A$  CMOS diodes. In addition, the effective doping concentration (Neff) and damage coefficient of both diodes had calculated. Our XRD results show some reductions in the crystalline size of the standard Si/SiO<sub>2</sub> wafers. But there is no change in the high resistivity silicon wafers. From AFM results show different defects in the surface of both in standard Si/SiO<sub>2</sub> and high resistivity silicon wafers.

School of Physics Academic Year 2019

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### LIST OF ABBREVIATIONS

ALICE	A Large Ion collider experiment
ALPIDE	ALICE Pixel detector
MAPS	Monolithic Active Pixel Sensor
QGP	Quark Gluon Plasma
SLRI	Synchrotron Light Research Institute
pALPIDEfs	prototype ALPIDE Pixel detector full-scale
$\mathrm{GeV}$	Giga electron-volts
CMOS	Complementary metal-oxide-semiconductor
DUT	Device Under Test
QCD	Quantun-Chromo Dynamics
LHC	Large Hadron collider
X0	Radiation length
LS2 LHC	Second long shut-down of LHC
ITS	Inner Tracking System
TPC	Time-Projection Chamber
MFT	Muon forward Tracking
HTF	Heavy Flavor Tracker
STAR	Solenoidal Tracker
RHIC	Relativistic Heavy Ion Collider

## LIST OF ABBREVIATIONS (Continued)

	TID	Total Ionizing Dose	
	NIEL	Non-Ionization Energy Lose	
	MAPS	Monolithic Active Pixel Sensor	
	TMEC	Thai Micro Electronics Center	
	TINT	Thailand Insitute of Nuclear Technology	
	SLRI	Synchrotron Light Research Institute	
	SUT	Suranaree University of Technology	
	FZ	Float zone method	
	RF	Radio frequency	
	$\mathrm{PH}_3$	Phosphine	
	$B_2H_6$	Diborane	
	Cz	Czochralski method	
	CVD	Chemical Vapor Deposition	
7	$\mathrm{E}_V$	Valence energy band	
	$E_C$	Conduction energy band	
	$\mathbf{E}_F$	Fermi energy band	
	Vbi	Buit-in potential	
	ADC	Digital Signal Converter	
	MEB	Multi-Event Buffer	
	SUE	Single Event Upset	
	LET	Linear Energy Transfer	

## LIST OF ABBREVIATIONS (Continued)

	$D_A$	Area diode
	$D_P$	Perimeter diode
	SRP	Spreading Resistance Profiling
	$\mathbf{R}_T$	Total measured resistance
	$\mathbf{R}_P$	Resistance of the probe
	$\mathbf{R}_C$	Contact resistance
	$\mathbf{R}_{SP}$	Spreading resistance
	$\mathbf{R}_M$	Material resistance
	STM	Scanning Tunneling Microscopy
	XRD	X-Ray Diffraction
	AFM	Atomic Force Microscopy
	SEM	Scanning Electron Microscope
	I-V	Current-Voltage
, ,	C-V	Capacitance-Voltage
	Neff	Effective doping concentration
	$\mathbf{I}_R$	Leakage current
	$\mathbf{J}_A$	Area current density
	$\mathbf{J}_P$	Perimeter current density
	$\mathbf{J}_C$	Corner current density
	$N_C$	Number of corner
	$I_{R0}$	Leakage current before irradiation

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## LIST OF ABBREVIATIONS (Continued)

	$\mathbf{I}_{R\phi}$	Leakage current after irradiation
	$K_I$	Current damage coefficient
	Q	Charge
	ρ	resistivity
	$B_0$	Boron before irradiation
	$B_{\phi}$	Boron after irradiation
	$\mathbf{R}_C$	Boron removal rate
	$\operatorname{Neff}_{\phi}$	Doping concentration after irradiation
	$\operatorname{Neff}_0$	Doping concentration before irradiation
	$\operatorname{Reff}_{\phi}$	Doping concentration removal rate
	$\mathbf{K}_C$	Capacitance damage coefficient
	φ	Irradiation dose
	C <sub>0</sub>	Capacitance before irradiation
2	$\mathrm{C}_{\phi}$	Capacitance after irradiation
	$V_R$	Reverse bias
	A	Area of the junction
	q	Elementary charge
	$\epsilon_{Si}$	the dielectric permittivity of silicon
	$J_{dA}$	Area diffusion current density
	$J_{gbA}$	Area bulk generation current density
	$W_A$	Area depletion width

### CHAPTER I

### INTRODUCTION

A Large Ion Collision Experiments (ALICE) is one of the detectors used at CERN (the European Organization for Nuclear Research) (Aamodt et al., 2008). The goal is to use heavy-ion collisions at the LHC (Large Hadron Collider) to study Quark Gluon plasma state (QGP). It is believed to be the state of matter at the early time of the universe. QGP is a state wherein quarks and gluons are not bound together in super-high matter density in infinitesimal volumes. The ALICE detector can be seen in figure 1.1.

In 2019-2020, the ALICE has been upgrading during the LHC Long Shutdown. One of the major component is the upgrade of the Inner Tracking Systems (ITS), the closest detector near a collision point, which consists of silicon sensors for tracking and vertexing of particle collider experiments. The starting materials for sensors fabrication are typically silicon wafers.

In this upgrade, there was a plan to replace the present tracking sensor by the Monolithic Active Pixel Sensors (MAPS)(Mager, 2016b), called the ALICE PIxel DEtector or ALPIDE. One of the ALPIDE design goals is to reduce its material budget from 1.14% to 0.3% for the inner layer and from 1% to 0.8% for the outer layer. The material budget of each ALPIDE sensor can be calculated from the radiation length of their components. The radiation length (X0) is the mean path length required to reduce the energy of relativistic charged particles, and it depend on either thickness (X/X0) or percentage of covered surface (X/ X0(%)) (Snoeys et al., 2017). Besides, the new sensor is required to be 50 microns thick to reduce the material budget with high resistivity around  $1 \text{ k}\Omega \cdot \text{cm}$  or greater to increase radiation tolerance. To achieve this goal, the MAPS technology was used since this technology is a combination of all sensor parts in the same piece, which able to reduce thickness (material budget) of the sensor. When the sensor fabricated using MAPS technology it can be damaged by radiation easier than the old type sensor. So the one essential thing is all sensors used must be radiation tolerant since sensors operate inside very harsh radiation environments.

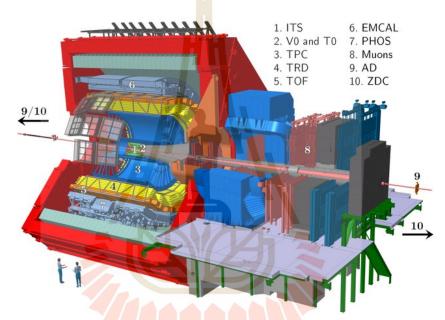


Figure 1.1 An ALICE experiment structure (ALICEwebsite, 2019).

According to the ALPIDE requirements, in addition to radiation-tolerance, there must also be several other properties as show in table 1.1 to allow a detailed study the Quark-Gluon Plasma (Paolo, 2017) in the future after the upgrade. Due to the above requirements, the silicon wafer, used as one of the sensor starting materials, and radiation effects of the sensor should be obtained and studied carefully.

#### 1.1 Inner Tracking System (ITS)

An Inner Tracking System (ITS) is the closest system near a collision point. It was designed for tracking particles after collision. The main idea of the ITS upgrade began when researchers foresaw limitations of the current ITS. They realised they needed to replace the existing one with a new model on the second long shutdown of LHC during 2019-2020 (LS2 LHC)(see figure 1.2). The new ITS had divided into seven cylindrical layers of strip silicon detectors placed coaxially around the beam pipe. It consists of three inner barrels and four outer barrels, which have different specifications. The inner barrel contains four layers, counting from the beam pipe, while the outer barrel contains four layers which are next layers from the inner, as shown in figure 1.3. The barrels are made of triangle structure called staves. Each stave contains many ALPIDEs. The layout of the alignment of ITS layers is shown in figure 1.2 (Abelev et al., 2014). Another purpose of the ITS upgrade is to bring these sensors as close to the collision point as possible (from 33 mm down to 22 mm) to detect the short-life particles. This implies that detector has to operate inside more hush radiation environment.

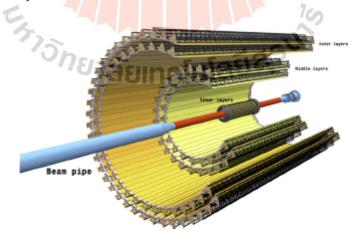


Figure 1.2 New ITS at LS2 2018/2019 (Abelev et al., 2014).

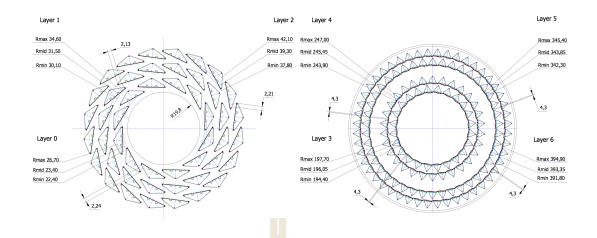


Figure 1.3 A new ITS cross-section at LS2 2018/2019 (Mager, 2016a).

#### **1.2** ALICE PIxel DEtector (ALPIDE)

Almost all pixel detectors that operated before upgrading in high-energy physics experiments are the hybrid type, which sensor part is separated from pixel readout chip. The sensor part is produced on silicon while the pixel readout chip is manufactured by using the standard CMOS process. Each charge collection diode (pixel cell) in the sensor is connected via micro-bump bonds to the corresponding cell in the readout chip as shown in figure 1.4.

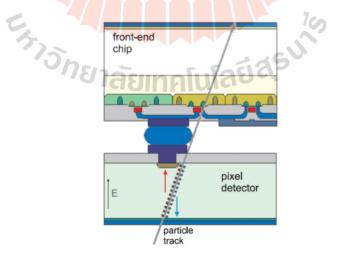


Figure 1.4 A cross-section through a typical hybrid pixel sensor. (Riedler, 2018)

The ALPIDE chip is implemented in a 180 nm CMOS Imaging Process

provided by TowerJazz (Senyukov et al., 2013) as a Monolithic Active Pixel sensor (MAPS). The idea of MAPS was first introduced into a Heavy Flavor Tracker (HFT) experiment at the Solenoidal Tracker (STAR), Relativistic Heavy Ion Collider (RHIC) in Sept 2013 (Abelev et al., 2014). In MAPS circuits can be fabricated on substrate with a high resistivity (> 1 k $\Omega$ cm) epitaxial layer on p-type substrate.

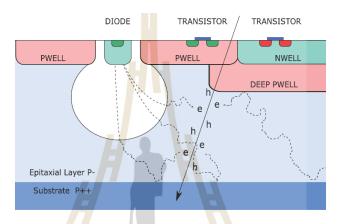


Figure 1.5 Structure design used in ALPIDE and its charge collection. (AL-ICEwebsite, 2019).

An ALPIDE sensor is a CMOS pixel sensor consisting of three major parts (figure 1.5). (i) SiO2 layer is a top layer of the sensor. It is the location where the electronic circuit of CMOS, such as gates and drains as well as a passivation layer to protect the surface of the sensor, are fabricated. (ii) An epitaxial layer is a middle layer of the sensor. By applying a reverse bias to the nwell-diode on top of the epitaxial layer, a depletion region is created inside the epitaxial layer under the nwell-diode. If there are high energy particles traveling through the sensor, electron-hole pairs will be created. These generated electrons are then moved and collected at the nwell-diode by thermal diffusion process (Shaw, 2017). (iii) The substrate is a highly P-doped (P++) silicon layer at the bottom of the sensor. At the junction of P-epi and P++, electrons will be reflected by the

Parameter	Inner barrel	Outer barrel
Max. silicon thickness	5	$50 \mu { m m}$
Intrinsic spatial resolution	$5~\mu{ m m}$	$10~\mu{ m m}$
Chip size	15  mm x 3	$0 \mathrm{mm} \; (\mathrm{r} \; \phi  \times  \mathrm{z})$
Max. dead area on chip	2 mm (r q	$\phi$ ), 25 $\mu {\rm m}$ (z)
Max. power density	$300 \frac{\text{mW}}{\text{cm}^2}$	$100 \frac{\mathrm{mW}}{\mathrm{cm}^2}$
Max. integration time	3	$30 \ \mu s$
Max. dead time	10% at 5	0 kHz Pb-Pb
Min. detection efficiency		99%
Max. fake hit rate	$10^{-5}$ [piz	$(\mathrm{kel} \cdot \mathrm{event}]^{-1}$
TID radiation hardness	700 krad	10 krad
NIEL radiation hardness	$10^{13} 1 \text{ MeV } n_{eq}/cm^2$	$3x10^{10}$ 1 MeV $n_{eq}/cm^2$

Table 1.1 The new ITS pixel sensor requirements (Abelev et al., 2014).

built-in voltage back to the nwell collection diode. For the LHC long shut down in 2018/2019, ALICE plans to construct a new ITS and Muon forward tracking (MFT). Hence ITS developers want to provide the new ITS ability to detect the low transverse momentum of heavy-flavour hadron, quarkonia, and low-mass dileptons. For the Pb-Pb collision, the detection sensitivity should be well obtained at 50 kHz (Kushpil, 2016). A development team attempted to develop a tracking sensor by using MAPS. Since the epitaxial layer of MAPS used in STAR RHIC, is 15  $\mu$ m thick with 400  $\Omega$  resistivity, from this idea, ALICE agrees to acquire properties of the new ITS (Abelev et al., 2014) as shown in table 1.1.

#### 1.3 High resistivity epitaxial silicon wafer

The high resistivity is essential for particle detectors because it have high radiation tolerance. Since one of the design goals for ALPIDE is to operate inside a high radiation environment more than 2700 krad before deterioration. Furthermore, it can act as a barrier between epitaxial layer and silicon substrate which affects the sensor performance collecting in electron generated from particle during operation. Therefore, ALICE had chosen "the towerjazz Complementary Metal-Oxide Semiconductor (CMOS)" technology with the transistor size of 0.18  $\mu$ m since it had most parts for sensitive area and fewer peripheral circuits (Abelev et al., 2014)

#### 1.4 Radiation damage of silicon detector

In high energy physics, detectors have to face with the high level of radiation environment of a high luminosity particle collider. The irradiation can change properties and induce noise while the semiconductor sensor is operating. Highenergy particles can produce two different types of effects that directly induce damage in the electronics part of the semiconductor device, displacement damage and ionization damage. The displacement damage occurs when atoms in silicon that are displaced from their normal lattices. For ionization damage, it is the damage in SiO<sub>2</sub> which is found inside detectors or silicon devices. These effects change the electrical properties while the detector is operating. More detail about the radiation damage effect will be described in Chapter III.

#### 1.5 Research objectives

Since the detection part of sensors consists of diodes, inn this work we would like to use diodes as a model for the simplest detector. The main goal of this thesis is to study radiation damages on different design diodes and use these results for designing new sensors in the future. Here, we focus only on the number of perimeters and corners of the diode.

To study the effect of radiation damage on electrical properties of the sensor, CMOS diodes were fabricated from a standard wafer at the Thai Micro Electronics Center (TMEC). These diodes called perimeter diode ( $D_P$ ) and area diode ( $D_A$ ). They were fabricated in a different number of perimeters and corners. The structure of diodes will be shown in section 5.1. The radiation damages were studied with several different radiation doses from electron and gamma sources at the Thailand Institute of Nuclear Technology (TINT). We have monitored the electrical properties changing by using Current-Voltage (I-V) and Capacitance-Voltage (C-V) characteristic. After that, the calculation of the radiation damage coefficients in silicon CMOS diodes has been carried out and the results are presented in Chapter V.

Other experiments were performed to examine the properties of the ultrathin silicon wafer for the new ALICE detector sensor or ALPIDE. The preliminary study of radiation damage and radiation tolerance of main materials inside ALPIDE are given in Appendix A and B.

To examine the properties of the ultra-thin silicon wafer for the ALPIDE, We use the Spreading Resistance Profiling (SRP) technique to examine Doping concentration and epitaxial layer depth, and the Four Point Probes (4PP) technique to define resistance geometry of the wafer surface. Then the Scanning Electron Microscope (SEM) is used to verify results by looking at its cross-section physically. Our results show that it is possible to obtain high resistivity wafers up to 1.6 k $\Omega$ cm with an epitaxial layer of 25 microns to be used as starting materials for the ALPIDE sensors. The results are presented in Appendix A.

Besides, we also investigate damages at the atomic structure and on the surface of the wafer, since radiation damages occur in surface and electronics circuits cause the charged particle to create electron-hole pair inside the SiO<sub>2</sub> and always change or trap between silicon and SiO<sub>2</sub> (Si-SiO<sub>2</sub>) interface. Therefore, the study to obtain more understanding about Si-SiO<sub>2</sub> interface after irradiation in the crystalline level plays an important role to understand radiation damage inside the particle detectors. Gamma and electron at different radiation doses were radiated on wafers to study the crystal and surface damages caused by irradiation. Then both wafers were studied by material characterization techniques, X-Ray Diffraction (XRD) and Atomic Force Microscope (AFM) before and after irradiation. The results are presented in Appendix B.

This thesis provided a brief description of several related theories and processes of silicon production in chapter II. Description of the radiation damage effects will be discussed in chapter III. Chapter IV provides the experimental techniques, experiment details, and method. The result of the effect of silicon diodes on irradiation is given in chapter V. A discussion and conclusion are reported in chapter VI.

# CHAPTER II BASICS ON SEMICONDUCTOR AND SILICON DETECTOR

Silicon strip sensors were widely used as detectors in modern high energy physics experiments for tracking the trajectories of charged particles after a collision. The silicon sensor with a very low material budget can offer precise spatial resolution and robust performance and operate inside an extremely high irradiation environment. Furthermore, the production technology of sensors follows common processes developed in the IC industry. They can be manufactured in mass quantities and kept the costs within reasonable amounts. The purpose of this chapter is to review the fundamental aspects of silicon technology and detector manufacturing concerning the challenges in the material requirements for detector fabrications.

## 2.1 Basic of silicon and semiconductor

#### 2.1.1 Silicon

Since sensors are made from silicon, in this section we will give a brief review of the physics of silicon. Silicon has a diamond lattice structure as shown in figure 2.1(a). Each atom in the diamond lattice is surrounded by four equidistant with a lattice spacing of 5.430710 Å (0.5430710 nm). A simplified two-dimensional diagram for the tetrahedron is shown in figure 2.1(b). Each atom has four valence electrons and shares these valence electrons with its four neighbors. The sharing of the electrons is known as covalent bonding.

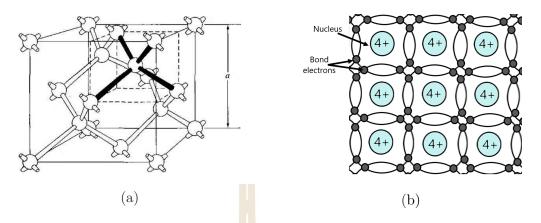


Figure 2.1 (a) A diamond lattice, and (b) tetrahedron bond of silicon.

The silicon element is a semiconductor material. To understand the chemical and electronic properties of the silicon, it is important to study the energy band structure. For an isolated atom, electrons in the atom have the only discrete energy level. When the atoms combine to become crystalline, the degenerate energy level will split into N levels due to atomic interactions.

### 2.1.2 Energy band

The detail of the energy band structures of crystalline solids silicon has been calculated by using quantum mechanics and shown in figure 2.2. The bands are separated by an area which designates energies that the electron cannot possess in the solid. This area is called the forbidden gap, or bandgap  $E_g$ . The top band is called the conduction band and the lower band is called the valence band, as shown on the left of figure 2.2 and 2.3.

10

The energy band diagram of three types of solid insulators, semiconductors, and conductors shown in figure 2.3. The insulator as shown in figure 2.3(a), there is a larger bandgap so the bonds are broken difficultly. Consequently, there is no free electron to move in the conduction band.

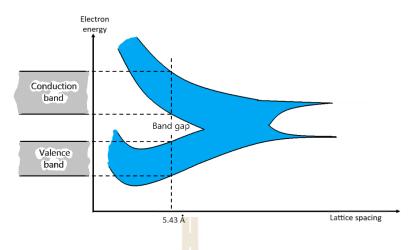


Figure 2.2 The schematic of energy bands formed by bringing together of several isolated silicon atoms.

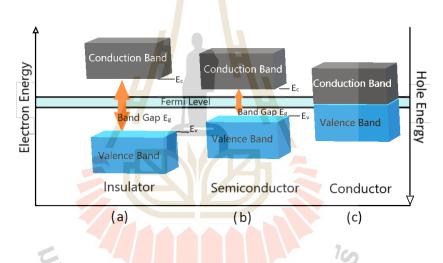


Figure 2.3 Simple model of electronic band structure in solids.

The valence band contains the electrons bound to a single nucleus of the solid: for example, in silicon, they form the covalent binding, which produces the inter-atomic forces of the crystal. The conduction band contains free electrons that can contribute to the electrical conductivity of the material. In an insulator, the forbidden gap is greater than 5 eV and it is very unlikely that an electron excited by thermal collision jumps from the valence band to the conduction band. In a semiconductor such as silicon, this bandgap is 1 eV and the electrons excited by the thermal collision can jump from the valence to the conduction band. The

electron leaves behind, in the valence band, an unoccupied place, called a hole, with a positive charge. Both carriers, the electron, and the hole can move in the electric field applied to the semiconductor, with different mobility. At the thermal equilibrium charge density of electrons and holes are equal.

In a semiconductor, the bond between neighboring atoms has moderately strong. As a result, thermal vibrations are able to break some bonds and generate free electrons inside the semiconductor material. Figure 2.3(b) shows that the band gap of the semiconductor is not as large as an insulator. Hence some electrons are able to move from the valence to the conduction band and generate holes in the valence band.

Figure 2.3(c) shows the conduction band has some region that overlaps with the valence band in conductors such as metal so that there is no bandgap. As a result, the electrons at the top of the valence band will move easily to a higher energy level when they gain an electric field. Therefore, current conduction in the conductor has flowed readily in conductors.

## 2.1.3 Extrinsic Properties of Doped Silicon

When dopant elements from Group III and IV in the periodic table, which have either one electron less or more than silicon, are added to silicon. It can change the number of charge carriers in the silicon as seen in figure 2.4.

The dopant from Group III called acceptors because they can accept an additional electron in the crystal lattice of silicon, and the dopant from Group IV are called donors because they can donate an additional electron.

The donor dopant usually are either phosphorus (P) or arsenic (As), the element from Group IV, that contain excess electron which will increase negative charge carriers. The negative charge has an energy state below the lower conduc-

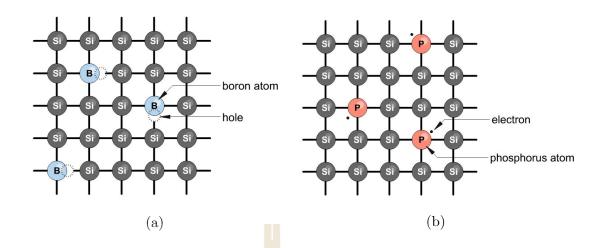


Figure 2.4 Silicon crystal lattice model of; (a) boron-doped or a p-type semiconductor, and (b) phosphorus-doped or an n-type semiconductor.

tion band as seen in figure 2.5. This type of doped silicon is called n-type silicon. Conversely, when we dope silicon with an acceptor usually using an element such as boron (B) from Group III that missing electrons will act as a positive charge called holes. These holes take place energy states slightly above the higher valence band energy as seen in figure 2.5. This type of doped silicon is called p-type silicon.

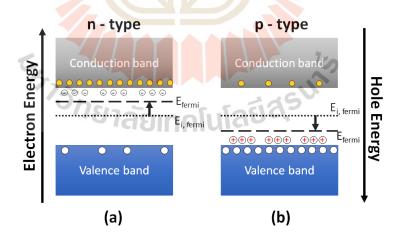


Figure 2.5 Schematic of the band energy of doped silicon and semiconductor. (a) n-type doped energy states below the lower conduction band, (b) p-type doped energy states are above the higher valence band.

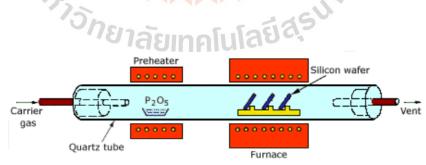
## 2.1.4 Doping method

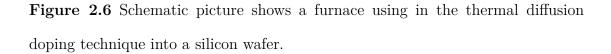
Doping is the input method of impurities element into the semiconductor crystal to intentionally change its conductivity due to deficiency or excess of electrons in silicon wafers or substrates. Two common methods for doping are thermal diffusion and ion implantation.

#### **Thermal Diffusion**

The diffusion doping technique is similar to the diffusion of molecules that diffuse from higher to lower concentration. For the silicon crystal, this is performed by heating the silicon wafers in furnaces together with dopant sources in the phase of gases, liquids, or solids.

To increase the quality and speed of the diffusion process, it depend on the following parameters, dopant element, the temperature in furnaces, concentration gradient, substrate type, and crystallographic orientation of the substrate. In the process, the wafer is structured by oxide masks and heated to about 900 °C. Then, the temperature that can activate the dopants element is a temperature of 1100 °C to 1250°C<sup>\*</sup>. A working parts of the diffusion doping technique implanter shown in figure 2.6.





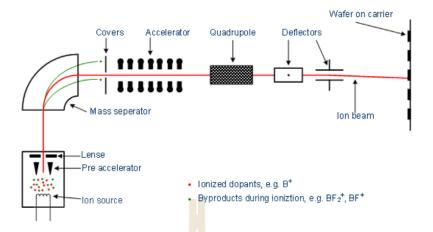


Figure 2.7 Ion implanter components (Halbleiter, 2015).

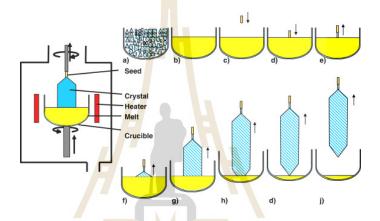
#### Ion Implantation

The ion implantation technique performs by accelerating charged dopants (ions) through an electrical field into a solid target to change some near-surface properties of each target. This technique is a standard fabrication process in semiconductor device manufacturing. It can be performed at room temperature. It can set the penetration depth very accurately by adjusting the voltage that applies to accelerate ions. Area that need not to be doped, will be covered by photoresist lack masks. Normally ion-implanted has low concentration of dopants and implantation depth is about one micron. An ion implantation technique implanter consists of working parts as shown in figure 2.7.

### 2.2 Silicon Crystal Growth Processes

## 2.2.1 Czochralski Silicon Growth

Czochralski pulling method is named after J. Czochralski, who determined the crystallization velocity of metals by pulling mono- and polycrystals against gravity out of a melt which is held in a crucible (Friedrich, 2016). However, the pull-from-melt method that widely used today was developed by Teal and Little in 1950 (Teal and Little, 1950). The Czochralski method (Cz) is the most important method for the production of bulk single crystals of a wide range of electronic and optical materials (Robert and Yoshio, 2008). Figure 2.8 shows a schematic of typical modern Cz grower for a large diameter silicon growth. Cz silicon growth consists of three major processes: (1) Seeding and necking process, (2) Body growth, (3) Tang growth/ termination.



**Figure 2.8** Process of the Czochralski method (a - b) Melt the polycrystalline feedstock, (c - d) Dip seed crystal into the melt, (e - j) Slowly lift off the seed called shouldering to growth silicon crystal and finally cooling down and removing of the crystal.(Friedrich, 2016)

The Czochralski method begins by feeding material that is put into a cylindrically shaped crucible and melted by resistance or radio-frequency heaters. Doping performed by adding dopants material as required for the needed resistivity in the rotating quartz crucible. After high purity polysilicon is melted, single crystal silicon seed is placed on the surface and slowly move upwards while it rotating. This draws the molten silicon after it which solidifies into a continuous crystal extending from the seed. A schematic diagram of a Czochralski-Si grower, called puller, is shown in figure 2.8. The puller consists of three main processes:

- Furnace is a process that includes a graphite susceptor, a fused-silica crucible, a heating element, a rotation mechanism, and a power supply as shown in figure 2.8.
- 2. A crystal-pulling mechanism that combines with a seed holder and a rotation mechanism (rotate in counter-Clockwise)
- 3. An ambient control consists of a gas source (such as argon), flow control, and an exhaust system.

Cz method was able to grow the vary huge silicon crystals rod with diameters of 450 mm and a weight exceeding 300 kg as shown in figure 2.9.



**Figure 2.9** Silicon crystal rod grew by the Cz method manufactured by courtesy of Siltronic AG company with a diameter of 300 mm and a weight of more than 250 kg. (Friedrich, 2016)

## 2.2.2 Float Zone Silicon Growth

The float zone method (FZ) was invented by Theuerer in 1962 and base on the zone-melting principle (Pfann, 1952). Float-zone silicon is a process for highpurity crystals grown more than the Czochralski process. This process provides very low concentrations of impurities such as carbon and oxygen. The schematic of the FZ process is shown in figure 2.10. A polysilicon rod is mounted vertically inside a growth chamber. The process performs under a vacuum or in an inert atmosphere. This method aims to turn polysilicon to monocrystalline silicon by melting. A needle-eye coil provides radio frequency (RF) power to the rod causing it to melt. FZ growth has two following main principles:

- 1. Molten zone is passed along the silicon rod
- 2. Melting the raw polycrystalline silicon as a starting material by an RF needle-eye coil and getting purified monocrystalline silicon

as shown in figure 2.10. At the beginning of the process, at the bottom-seed of FZ, the small seed crystal is made contact with the drop of melted silicon at the tip of the polysilicon rod. The shape of the molten zone and crystal diameter is adjusted by the RF power of the coil and the travel speed during the growth process and detected by infrared sensing. Modern FZ machines are now capable of accepting feed rods up to 2 m long with a weight between 60 and 100 kg (Augustin et al., 2012).

During the FZ doping elements can be added by flowing the gas state material such as diborane ( $B_2H_6$ ) for the p-type or phosphine ( $PH_3$ ) for the n-type semiconductor (Robert and Yoshio, 2008). FZ silicon is usually used in detector and power electronic components but FZ crystal has a diameter only 100-125 mm, so it can not be a substrate for a large scale sensor. Silicon wafer from FZ growth

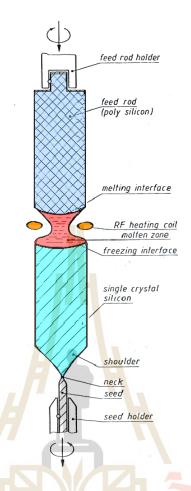


Figure 2.10 Float zone (FZ) silicon crystal growth technique (Laube, 2012).

technique can provide a diameter of 25 - 150 mm and resistance between 0.01 - 100,000  $\omega$ cm (Augustin et al., 2012). Details of the FZ method are discussed by Robert and Yoshio (Robert and Yoshio, 2008).

## 2.3 Epitaxial Growth

The epitaxial silicon layer is the layer grown on a single crystal silicon substrate commonly by chemical vapor deposition (CVD). The resulting grown layer is an exact crystalline extension of the substrate. The advantages of an epitaxial layer over the silicon substrate are to improve the performance of the bipolar device, protection of latch-up in CMOS circuits, and easier to control doping concentration.

In commercial, they usually use four chemical sources of silicon types for epitaxial deposition as following:

- 1. Silane  $(SiH_4)$
- 2. Trichlorosilane  $(SiHCl_3)$
- 3. Silicon tetrachloride  $(SiCl_4)$
- 4. Dichlorosilane  $(SiH_2Cl_2)$

The three major conditions that relate to the growth rate of an epitaxial layer consist of 1) the chemical sources used for deposition; 2) the deposition temperature, and 3) the mole fraction of reactants. For more details and all of the processes can find in (Wolf and Tauber, 2000).

## 2.4 The basic of p-n junction

The basic structure of silicon detectors is the p-n junction. The p-n junction occurs when we bring semiconductor n-type and p-type in contact to each other as shown in figure 2.11. At the p-n junction, the p-type near the valence energy band  $(E_V)$  that rich of holes is lowered, while the n-type near conduction energy band  $(E_C)$  that filled with electrons is lift higher until there are equal to Fermi energy level  $(E_F)$  as shown in figure 2.11.

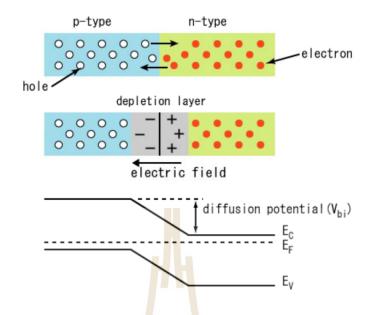


Figure 2.11 A simplified model of non-bias structure in p-n junction.

Finally, the p-n junction will create the depletion layer which empties electrons and holes. The depletion layer behaves as a barrier called built-in potential  $(V_{bi})$  to stop electron and hole moving across the junction. When applying a voltage like a figure 2.12, electrons in n-type and p-type semiconductor will attract electrons and holes respectively to move across the junction. This allows the current to flow through the junction called forward biasing.

If we apply a voltage as seen in figure 2.13, it is called a reverse bias. Because the p-type semiconductor is in contact with the negative side of the applied voltage. Holes in the p-type material are moved away from the junction which increases the thickness of the depletion region. Therefore, no current will flow across the p-n junction until the electric field by applied voltage is so high that the diode breaks down. It means that the depletion region expands fully through the p-n junction and we call this voltage a "break down voltage". Typically in a reverse bias, there exists very small electric current to leak across the p-n junction called leakage current.

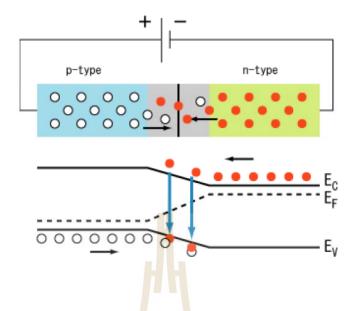


Figure 2.12 A simplified model of forward bias structure in p-n junction.

## 2.5 Monolithic Active Pixel Sensor (MAPS)

Monolithic Active Pixel Sensor (MAPS) is a combination of a sensing layer with an electronic read-out for reducing a material budget (less thickness) and large charge collection. There are N-well diode, P-well, P-MOS transistor, N-MOS transistor, and Deep p-well. The function of an N-well diode is to keep ionized electrons that generate from ionization. P-well is used for producing depletion region to distinguish the ionized electrons from a background. The NMOS-transistor and the P-MOS transistor are the electronic circuits located on top of the sensor used as Analog to Digital signal Converter (ADC) and logic gate. The deep P-well is designed to shield PMOS and NMOS-transistor from leaking electrons. During its operation, a back-bias voltage ( $V_{back-bias}$ ) is applied to generate the depletion region for keeping out the background electron in the medium (Snoeys et al., 2017) as shown in figure 2.14. Whenever high-energy particles pass through an epitaxial layer (in a silicon die in MAPS or sensitive volume), they ionize and generate electron-hole pairs in the epitaxial layer. The wafer is doped for high resistivity

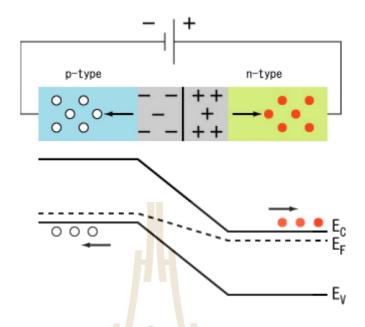


Figure 2.13 A simplified model of reverse bias structure in p-n junction.

 $(> 1k\Omega \cdot cm)$  to reduce charge carrier trapping in the silicon layer (making a charge losing in an electronics read-out) with a sufficient radiation tolerance. Then electrons from ionization move as random motion (non-steady moving direction) by diffusion until they reach the depletion region where there exists an electric field to induce electron movement toward the N-well diode. Whenever particles pass through a silicon die, an incoming particle always loses the energy from ionization.

## 2.6 ALPIDE principle

The ALICE Pixel Detector (ALPIDE) sensor is designed for a new Inner Tracking System (ITS) and constructed by using CMOS Monolithic Active Pixel technology. The ALPIDE chip is measured 15 mm (width)  $\times$  30 mm (length) and contains a matrix of 512  $\times$  1024 pixels, (width  $\times$  length) 29.24  $\mu m \times$  26.88  $\mu m$ for any pixel as shown in figure 2.15. A peripheral circuit of 1.2 mm  $\times$  30 mm includes the control and read-out functionality (Keil, 2017).

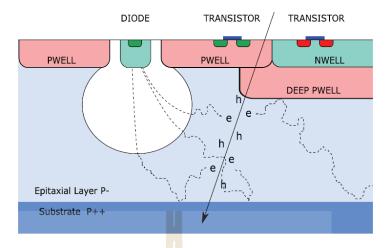
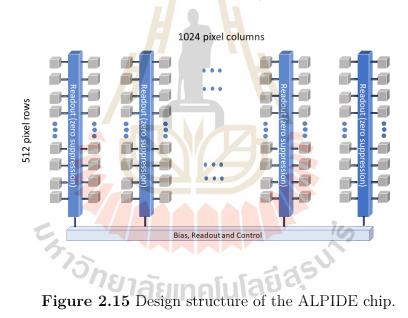
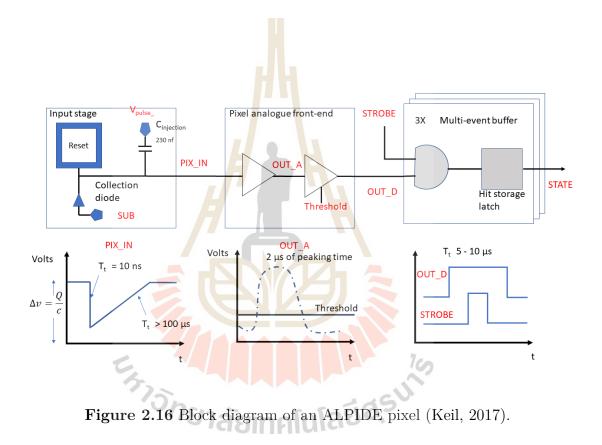


Figure 2.14 A cross-section of Towerjazz Monolithic Active Pixel Sensor (MAPS) (Mager, 2016a).

In each ALPIDE pixel, it consists of a digital section, a front-end amplifying, a sensing node and shaping stage, and a discriminator.

For a digital section, there are the following parts, three-hit storage registers (Multi-Event Buffer or MEB), pulsing logic, and a pixel masking register. And front-end and discriminator continuously operate and characterize a non-linear response. Their transistors are biased in low inversions with the power consumption about 40 nW. For a front-end output, there is an order of 2  $\mu$ s of a peaking time. A discrimination pulse has a 10  $\mu$ s of typical duration time. A global shutter (STROBE signal) can be used to control a discriminated hit in a storage register. A STROBE is pushed to the selected cell whenever the front-end is over a threshold. A pixel hit is sent into one of three in-pixel memory cells. The common STROBE signal is produced from the peripheral circuit. The STROBE signal is used to control the storage of the pixel hit information in the pixel event buffers. An external command (TRIGGER) can trigger a level of the internal STROBE signal. Because the duration of the STROBE signal can be programed, a pulse injection capacitor is constructed for test charge injection in the input of the front-end for all pixels. A digital-only pulsing mode is also available to force the logic writing in the pixel memory cells. The pulsing patterns are entirely able to program. The readout of pixel hit data named Priority Encoder from the matrix which consists of 512 instances of this circuit. There is one circuit for every two-pixel columns. The Priority Encoder performs the first-pixel periphery address with a hit in its double column and selects a pixel according to a hardwired topological priority. A hit on a pixel is chosen during a hit transfer cycle. A pixel address is provided and transmitted to the periphery circuit, and the in-pixel memory element is finally reset (ALICE ITS upgrade collaboration, 2016).





# CHAPTER III RADIATION DAMAGE EFFECTS

This chapter starts with the description of the basic radiation damage mechanisms that can produce radiation damage in semiconductor devices at least two different types that directly affect electronics, ionization damage and displacement damage. Sometimes, radiation damage in silicon detectors can roughly be divided into surface and bulk damage. Damage in solid-state detectors on a macroscopic scale causes an increase of leakage current in sensors which affects an increase in noise. Besides, the damage in a semiconductor can change several properties of electronics device such as the material resistivity, reduce the ability of collected charge due to the charge carrier trapping mechanism, and the decrease of the carrier's mobility and their lifetime. The degradation of each property of diode and MOS devices in particle detector is caused by radiation-induced surface damage and effects at the Si-SiO<sub>2</sub> interface. Furthermore, radiation can induce bulk damage inside the material bulk, it causes the permanent change in properties of the device. In this chapter, the effects are briefly summarized.

## 3.1 Radiation effect in semiconductor devices

High energy particles can produce radiation damage in semiconductor devices at least two different types that directly effect electronics, ionization damage and displacement damage. Radiation damage can be classified into two types which are surface damage and bulk damage.

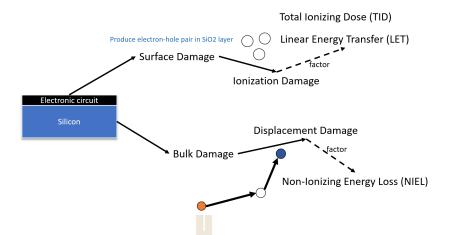


Figure 3.1 Diagram of surface and bulk damage in silicon detector cause by high energy particle irradiation.

## 3.1.1 Surface damage

Ionization create free electron-hole pair in the  $SiO_2$  layer by disrupting electronic bond, which can cause either short-term or long-term ionizing damage. One importance of short-term damage is the Single Event Upset (SUE). It occurs when a single high-energy particle generates a critical node of the device, after that leaving behind an ionized track passing through the storage capacitor. It causes the device to work incorrectly, but short-term damage effect can be back to normal by resetting the device or software correction. While long-term ionization damage occurs from the primary ionizing particles producing electrons and holes along their tracks. The generated electrons are highly mobile in comparison with the holes when produced in  $SiO_2$ . These holes become trapped and act as fixed positive charges. The most common ionizing radiation effects in the oxide are charge trapping as shown in figure 3.2.

The trap that occurred in  $SiO_2$  will confine the movement of electrons and holes. Traps play an important role in the operation of various electronic devices since they are able to carry an electrical current depending on the mobility of

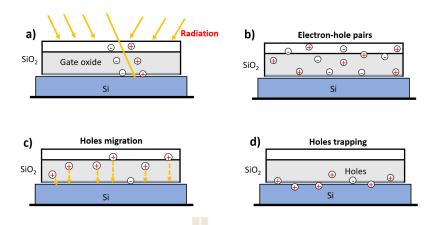


Figure 3.2 Particle generates a critical node of the device: a) when radiation hit on the sensor, b) radiation generate electron-hole pair, c) holes migration from SiO<sub>2</sub> to Si bulk, and d) holes trapping between Si and SiO<sub>2</sub> interface.

electrons and holes through that solid. Charge in the oxide, leads to the formation of recombination centers and field effects, particularly at  $Si-SIO_2$  junction. A trap can decrease mobility an electron or hole and prevent its recombination of an electron-hole pair. Charge carriers can be released from traps by the activated energy, such as annealing the semiconductor device with light or by heating it.

The quantity of energy deposited in the material through ionization interactions is determined by the Linear Energy Transfer (LET) function in the unit of MeV-cm<sup>2</sup>/g, given by (Holmes-Siedle and Adams, 1993)

$$LET = \rho_m^{-1} \frac{dE}{dx},\tag{3.1}$$

$$-\frac{dE}{dx} = 2Pq^4 Z_1^2 Z_2 N_{at} \frac{M_2}{M_1} \frac{1}{E} ln(\frac{4E}{E_{eh}}), \qquad (3.2)$$

where  $\rho_m$  is the density of the material, P is the stopping number of the material, q is the electron charge in absolute value,  $Z_1$  and  $Z_2$  are the atomic charges of the incident particle and the target material,  $N_{at}$  is the atomic density of target,  $M_2$  is the corresponding atomic mass of the target,  $M_1$  and E are the mass and energy of the incident particles and  $E_{eh}$  is the mean ionization energy.

## 3.1.2 Bulk damage

Bulk damage from radiation in silicon leads to limit the use of silicon detector in high radiation environments at the CERN-LHC or in space. The bulk or displacement damage is caused by the non-ionizing energy loss (NIEL) interactions of the incident particles with the nuclei of the lattice atom. It is giving rise to atoms that are displaced from their usual lattice positions, leaving behind a vacancy shown in figure 3.3. As a result, it will create a Frenkel pair: a silicon self-interstitial (I) and lattice vacancy (V). If there is only one atom disorder in a crystalline lattice, it is called a point defect.

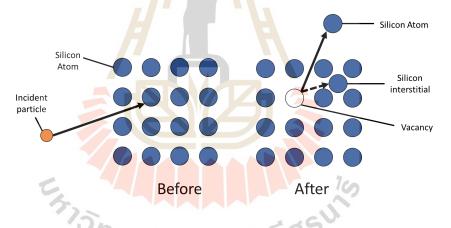


Figure 3.3 Schematic of vacancy and silicon interstitial formation cause by high energy particle irradiation.

To compare the damage caused by each type of particles with different energies, radiation damage is indicated with the NIEL and had calculated by Vasilescu and Lindstroem(Vasilescu and Lindstroem, 2016) as shown in figure 3.4. They used equivalent fluence of 1MeV neutrons as reference particles. NIEL can be calculated for electrons, protons, neutrons, and etc., using the following relation (Dale and Marshall, 1991)(Xapsos et al., 1994)

$$NIEL = \left(\frac{N}{M_2}\right) \sum_i \sigma_{di}(E) E_{ri}(E), \qquad (3.3)$$

where N is Avogadro's number (6.02257x10<sup>23</sup>),  $M_2$  is the gram atomic mass of the target,  $\sigma_{di}(E)$  and  $E_{ri}(E)$  are the cross section and average recoil energy for each incident particle energy (E) of primary knock-on atoms and for each kind of nuclear interaction (i) contributing to the energy loss.

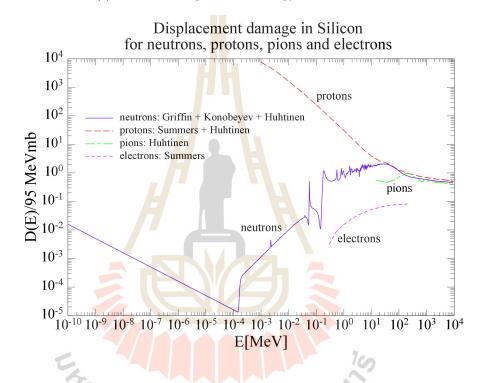


Figure 3.4 Displacement damage with energy of in silicon for neutrons, protons, pions and electron. (Vasilescu and Lindstroem, 2016)

In contrast to ionization, bulk damages are mostly permanent damage. For damaging silicon atom from its lattice position, it has to use a minimum of 25 eV of recoil energy. Each particle type requires different energy to provide recoil energy in a collision, electrons need the energy at least 260 keV, while protons and neutrons require only 190 eV because of their higher masses. With these amount of energy it will create isolated displacement, and leave behind vacancy-interstitials pair as shown in the figure 3.3. The ionization plays an important role in the surface and interface (Si-SiO<sub>2</sub>) component, while displacement damage mainly impacts the bulk properties.

## 3.2 Changes in silicon detector properties by radiation damage

Radiation damage can induce electrical defects in a silicon detector with energy levels in the silicon bandgap which directly impact on the device performance in various ways. Generally, the impact on the detector performance can be described by the leakage current and the effective concentration of the defect (*N*eff) (Moll, 2018). Three main effects on the detector performance can be identified and are discussed in the following.

### 3.2.1 Leakage current

The leakage current occurs while reverse biasing. More details of components and characterized methods will be provided in the next chapter. The leakage current in a reverse-biased junction depends on the concentration of generation centers. It is observed in the experiment that the leakage current of reverse biasing detector increases linearly with radiation fluence. The impact of irradiation damage on leakage current can be described by a current damage coefficient  $(K_I)$ . The relation of the leakage current before  $(I_{R0})$  and after  $(I_{R\phi})$  on the damaging particle fluence, given by (Moritz et al., 2018)

$$I_{R\phi} = I_{R0} + K_I \phi. \tag{3.4}$$

Therefore,  $K_I$  at each of  $\phi$  is

$$K_I = \frac{I_{R\phi} - I_{R0}}{\phi}.$$
 (3.5)

The increase of leakage current leads to an increase of noise in the amplifiers and an increase in power consumption.

## **3.2.2 Effective Doping concentration** (Neff)

Inside the irradiation environment, when donors are removed, it is left with holes that act as defects generated throughout the bulk of silicon. This effect leads to a decrease in the doping concentration inside the silicon bulk called the effective doping concentration, Neff. It can be defined by the relation of effective doping concentration damage coefficient (Reff) that will be discussed in chapter V.

## 3.2.3 Trapping

When ionizing particles or photons pass through p-n or MOS devices it generates charge carriers in the depleted region inside the bulk of the silicon sensor. Afterward, charge carriers travel to the electrodes of the sensor and become the signal. In case a charge carrier is trapped into a defect level that occurs from radiation damages. If the charge carrier cannot escape within the signal collection time of the sensor, this phenomena lead to loss of the charge which reduces the corresponding sensor signal.

All of these effects mentioned in this chapter can generate degradation in particle detectors at the operation by changing their electrical and structural properties. As a result, the particle detector must concern with its radiation hardness by testing it before really use. In the next chapter, the experiment details which we use in our study to test the particle detector with radiation will be provided.

## CHAPTER IV

## EXPERIMENTAL DETAILS

To characterize silicon wafers and study electrical properties changing before and after irradiation, several techniques have been used. All of the techniques that have been used in this study will be discussed in this chapter. Details of the research procedure are also provided.

## 4.1 Electrical characterization techniques

## 4.1.1 Four-point probe and wafer mapping

The four-point probe is a technique for measuring the resistivity of materials. By applying a current through two outer probes while measuring the voltage by inner probes as shown in figure 4.1 it allows us to measure the resistivity of materials. This technique can measure either sheet or bulk resistivity.

# Sheet resistivity measurement

The sheet resistivity  $(R_{sh})$  of the surface is easy to measure experimentally using a "four-point probe". The junction between the n-type and p-type materials behave as an insulator layer and while the measurement must be performed in the dark. By using the voltage readings from the probe (Smits, 1958), we get

$$R_{sh} = \rho = \frac{\pi}{\ln(2)} \frac{V}{I} s = 4.532 \frac{V}{I} s, \qquad (4.1)$$

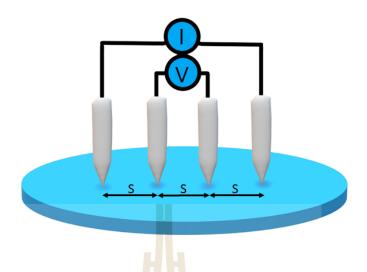


Figure 4.1 Four-point probe measurement by applying a current through two outer probes while measuring the voltage by inner probes.

where  $\rho$  is the sheet resistance, V is voltage between inner probes, I is the current through outer probes, and s is the probes spacing.

So in typical measurement, the current is set to 4.53 mA for easy reading the voltage in mV which is corresponding to its sheet resistivity.

#### Bulk resistivity measurement

The measurement of bulk resistivity  $(R_{bulk})$  is similar to that of sheet resistivity except that a resistivity are reported in cm<sup>-3</sup>. We can calculate by equation;

$$R_{bulk} = \frac{\rho}{t} = \frac{\pi}{\ln(2)} \frac{V}{I} t = 4.532 \frac{V}{I} t, \qquad (4.2)$$

10

where  $\rho$  is the sheet resistance, V is voltage between inner probes, I is the current through outer probes, and t is the wafer thickness. But the above formula gives the good results when the wafer thickness less than half the probe spacing(s) (s is shown in figure 4.1) (t < s/2) (Dieter K., 2006). For high-thickness samples, the formula becomes

$$\rho = \frac{V}{I} \frac{\pi t}{\ln(\frac{\sinh(\frac{t}{s})}{\sinh(\frac{t}{s_{1}})})},\tag{4.3}$$

where s is the probe spacing.

There are several sheet resistance wafer mapping techniques such as fourpoint probe sheet resistance, modulated photo-reflectance, and optical densitometry (Schroder, 2006). But, the configuration- switched four-point probe method is commonly used. In our work, we have learned and used this technique from experts at Thai Microelectronic Center (TMEC). This method allows as to characterize ion implantation, diffusion, poly-Si films, and metal uniformity of the wafer.

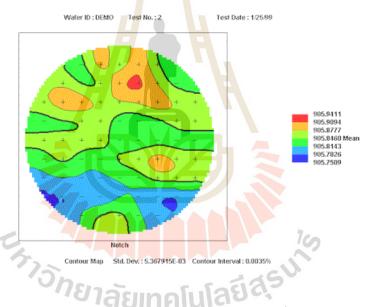


Figure 4.2 Four-point probe contour maps example (Four Dimensions, 2008).

## 4.1.2 Capacitance-Voltage (C-V) characteristic

The capacitance-voltage technique relies on the fact that the width of the depletion width of the semiconductor junction device depends on the applied reverse voltage. The definition of capacitance is the change in charge (Q) in a device that occurs when it also has a change in the voltage (V). The differential

or small-signal capacitance is defined by

$$C = \frac{dQ}{dV} = qA\frac{d}{dV}\int_0^W N_A dx = qAN_A(W)\frac{dW}{dV},$$
(4.4)

where q is the electron charge (1.6 x  $10^{-19}$  C), A is a cross-section area of band bending in a Schottky barrier, W is the depletion region width and  $N_A$  is the acceptor doping concentration. C-V Characterization is a technique for characterizing semiconductor materials and devices. It is a nondestructive method to measure the doping concentration of  $N_A(W)$ . By varying the applied voltage, first, we measure the capacitance of the sample then plot the graph between capacitance and voltage. The depth profile of  $N_A(W)$  inside the silicon bulk can be understood (figure 4.3) from the plot of C-V curve using the formula

$$N_A(W) = -\frac{C^3}{q\epsilon_{Si}A^2\frac{dC}{dV}} = \frac{2}{q\epsilon_{Si}A^2\frac{d(1/C^2)}{dV}},$$
(4.5)

where q is the electron charge (1.6 x  $10^{-19}$  C),  $\epsilon_{Si}$  is the permittivity of free silicon,  $\epsilon_0$  is the permittivity of free space(8.854x10^{-14} F/cm), A is the contact area, V is the apply voltage and C is the capacitance.

We can calculate the depletion depth d to get the depth profile of doping density from (Dragicevic et al., 2013)

$$W = \frac{\epsilon_{Si}A}{C},\tag{4.6}$$

where W is the depletion region width. While voltage is applied during the probe tip and substrate contact together, the depletion region near the interface will occur as shown in figure 4.3.

Equation (4.5) and (4.6) are important relations to obtain doping profiling. From the slope dC/dV of the C-V curve or the slope  $d(1/C^2)/dV$  of a  $1/C^2$  - V curve the doping density of the semiconductor device can be obtained. The depletion width (W), which expands when applying voltage, is obtained from equation (4.6).

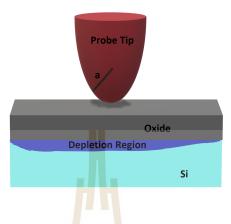


Figure 4.3 Schematic of the probe tip in the C-V measurement technique.

#### Effective doping concentration (Neff)

Inside the irradiation environment, both donors are removed and acceptorlike defects are generated throughout the bulk. This effect leads to a decrease of the doping concentration inside the silicon bulk called the effective doping concentration Neff as it follows

$$Neff = |N_D - N_A|, \tag{4.7}$$

where  $N_A$  is the acceptor concentration in the n side region of the junction and  $N_D$  is the dornor concentration in the p side region of the junction. Neff is related to the resistivity ( $\rho$ ) of the material by

$$\rho \approx \frac{1}{q\mu N \text{eff}}.$$
(4.8)

Neff can be measured from C-V characterization. In the beginning, when applying voltage, if sensors behave according to theoretically predicted the depletion voltage

will increase with the Neff. For high-resistivity sensors like ALPIDE with low initial donor density and low fluence, they will reach the inversion point faster than that of the low resistivity sensors.

## 4.1.3 Current-Voltage (I-V) characteristic

Current-voltage characteristic (I-V), is a measurement technique that observes the relationship between the applied voltage of an electrical device and the current flowing through it by the I-V curve. It is the common use technique to determine electrical device properties in a circuit. I-V measurement is operated by sweeping applied voltages to the device. The current flowing pass the device is measured, at each applied voltage. In figure 4.4 shows an I-V measurement of an ideal diode, the applied voltage is measured by a voltmeter that connected parallelly to the diode, and the current is measured by a series connection ammeter.

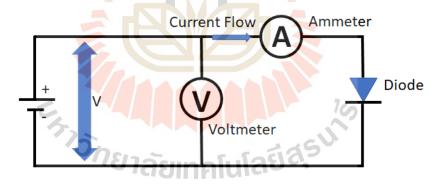


Figure 4.4 Schematic of Circuit for an I-V measurement of an ideal diode.

For a diode which just allows current flowing through in one direction. The I-V curve of the diode can be seen in figure 4.5. When we apply positive voltages the curve will rises exponentially caused by the current can free flow through the diode, this event is called forward bias. On the other hand, if we apply negative voltages or reverse bias, the current will nearly be at zero the current that occur called leakage current. After the reverse bias is sufficiently large will effect the diode to become conductive to negative current called breakdown voltage.

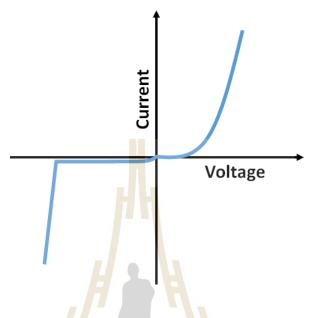


Figure 4.5 I-V curve of an ideal diode.

## Leakage current

While reverse biasing, there will be a small current flowing through a p-n junction called the leakage current  $(I_R)$ , as shown in figure 4.5. By considering in figure 4.5 the total leakage current  $(I_R)$  is a linear combination of the different geometrical current component and given by [7]

$$I_R = AJ_A + PJ_P + NJ_C + I_{par}, (4.9)$$

$$J_A = J_{dA} + J_{gbA},\tag{4.10}$$

where  $J_A$  (A/cm<sup>2</sup>) is the area current density scaling with the area of the diode or p-n junction (A),  $J_P$  (A/cm) is the perimeter current density defined by the perimeter of the diode (P),  $J_C$  (A/corner) is the corner current density defined with the number of diode corners ( $N_C$ ),  $I_{par}$  is the parasitic sample-independent system leakage,  $J_{dA}$  is the area diffusion current density, and  $J_{gbA}$  is the area bulk generation current density.  $J_{gbA}$  is given by

$$J_{gbA} = \frac{Aqn_i W_A}{\tau_g} \tag{4.11}$$

Then  $J_A$  can be rewritten as

$$J_A = J_{dA} + \frac{Aqn_i W_A}{\tau_g},\tag{4.12}$$

Equation 4.12 shows that a linear between  $J_A$  and  $W_A$  will be obtained in case  $J_{dA}$ is bias independent and  $\tau_g$  is constannt along  $W_A$  The intercept at  $W_A = 0$  gives  $J_{dA}$ , while the slpoe yields  $(qn_i/\tau_g)$  from that plot (Murakami and Shingyouji, 1994).

## 4.1.4 Spreading Resistance Profiling(SRP)

Spreading Resistance Profiling (SRP) is the main technique to study the silicon wafer at TMEC. This method has been in use since the 1960s (Schroder, 2006). It is mainly used today to measure resistivity and dopant density depth profiles. The concept of SRP is illustrated in figure 4.6. During the measurement, two precisely aligned probe tips move along the beveled surface of the prepared semiconductor and measure the resistance inside the material bulk at each position. The different components of the total measured resistance  $(R_T)$  are the resistance of the probes  $(R_P)$ , the contact resistance  $(R_C)$ , the spreading resistance  $(R_{SP})$ and the resistance of the material  $(R_M)$ (Treberspurg et al., 2012)

$$R_T = 2R_P + 2R_C + 2R_{SP} + R_M. (4.13)$$

This technique has very high dynamic range  $(10^{12} - 10^{21} \text{cm}^{-3})$  and can give profiling at very shallow junctions into nanometer-scale (Schroder, 2006). SRP can

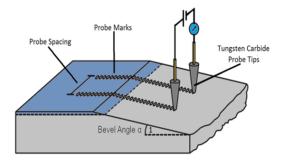


Figure 4.6 Measurement of SRP: two probe tips are stepped along the beveled surface of the prepared sample, measure resistance inside the material bulk.

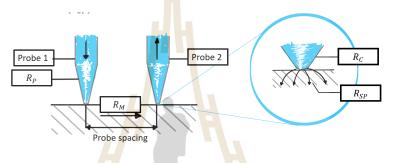


Figure 4.7 A combination of resistances that occurring from two probes when measuring resistance with the SRP technique.

also directly measure the resistivity inside the bulk of the material if the samples were cut to open inside before measurement. In SRP measurement, the resistance is a function of depth. It is determined by applying a voltage ramp across two probes where other resistances except spreading resistance are controlled. The measured resistance is dominated by spreading resistance effect as shown in figure 4.8 and 4.7. During measurement, the current concentrates at the small probe tips of radius 5  $\mu$ m and spreads out radially into the material of resistivity ( $\rho$ )

$$R_{SP} = \frac{\rho}{2a} \tag{4.14}$$

where a is the radis of probe tips.

There are two reasons in this technique which make it very convenient

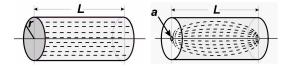


Figure 4.8 Spreading resistance effect.

(Treberspurg et al., 2012):

- $R_{SP} = \frac{\rho}{2a}$  is strongly correlated to the probe tip radius. By decreasing the radius, very high resistance values can be measured and the influence of  $R_C$  and  $R_M$  are reduced.
- The measured resistance is just slightly influenced by fluctuations of the probe spacing, the alignment of the probes is not critical.

In SRP measurement, the resistance is a function of depth. It is determined by applying a voltage ramp across the probes where the measured resistance is dominated by spreading resistance effect as shown in figure 4.8. During measurement, the current concentrates at the small probe tips of radius 2  $\mu$ m and spreads out radially into the material of resistivity  $\rho$ . The sample preparation for SRP measurement is very important part prior to the measurement since it is associated with the accuracy of measurement (Clarysse et al., 2000).

## 4.2 Crystallographic structure and morphology analysis

## 4.2.1 X-Ray Diffraction

X-ray diffraction (XRD) is a measurement technique used to identify the crystalline materials by the diffraction phenomena of x-ray in the crystalline material. It can express information on the crystal structure and crystalline phases inside the material. In XRD measurement, X-ray diffraction will arise only when the Bragg requirement is satisfied as shown in figure 4.9

$$n\lambda = 2d\sin\theta,\tag{4.15}$$

where  $\lambda$  is the x-ray wavelength, d is the interplaner spacing,  $\theta$  is the Bragg diffraction angle, and n is the integer giving the order of the diffraction.

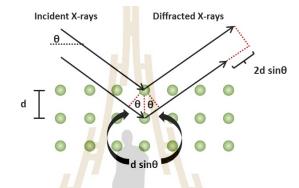


Figure 4.9 Schematic diagram of Bragg's law of X-Ray Diffraction in X-ray diffraction measurement.

The advantage of XRD is that it can characterize crystalline materials, determine unit cell dimensions, measure sample purity, and also identify finegrained structure of minerals. However, the XRD technique requires a standard reference of inorganic compounds such as the distance between planes of atoms (dspacing) that gives the diffraction patterns and plane directions (hkls). If there is no standard reference in the database, we have to make the reference by ourselves. For some kind of materials or novel bonding, we may have to make it into a powder before doing the XRD measurement.

## 4.2.2 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a scanning probe microscope. AFM carries on three-dimensional characterization with a subnanometer resolution (Singer et al., 2019). In the beginning, AFM was developed to overcome a basic deficiency of Scanning Tunneling Microscopy (STM), it was only able to image conducting or semiconducting surfaces. At present, AFM has more options for surface imaging, such as biological samples, ceramics, glass, composites, and polymers. Most of Atomic Force Microscopes use a laser beam deflection system which is the system that measures reflected laser from the back AFM probe (or lever) onto a positionsensitive detector as shown in figure 4.10. AFM tips and cantilevers are typically micro-fabricated from Si or Si<sub>3</sub>N<sub>4</sub>. The typical tip radius is only a few nanometer.

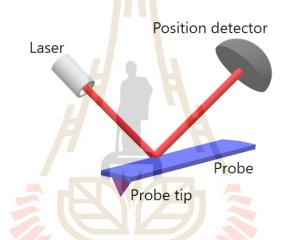


Figure 4.10 Laser beam deflection from the tip by for the atomic force of sample.

The AFM measurement principle relies on the forces between the tip and sample, these forces affect AFM imaging. The force is not measured directly but calculated by measuring the deflection of the probe tip (figure 4.10), by using Hooke's law gives

$$F = -kx, \tag{4.16}$$

where F is the force, k is the stiffness coefficients of the probe, and x is the distance of probe bending from the origin.

## 4.3 Research procedure

## 4.3.1 Epitaxial layer thickness measurement

The SRP was used to measure resistivity at a certain depth. It can find dopant concentration and epitaxial layer thickness. Then, we use SEM results to confirm epitaxial layer thickness with SRP. Before SRP measurement, five samples were prepared from the five different areas (top, bottom, left, right and center) of the silicon wafer by Max  $\mu$ m elite (cutting machine) to size  $3x1 \text{ cm}^2$ (figure 4.11). Then we mount them with melted wax on the bevel block 1° (figure 4.12). This part is a very important part prior to the measurement since it is associated with the accuracy of measurement.



Figure 4.11 Cutting the silicon wafer in  $3x1 \text{ cm}^2$ .

Next, we polish the sample with a polishing wheel together with a diamond polishing compound of the size 1  $\mu$ m for coarse grinding and size 0.25  $\mu$ m for fine grinding (figure 4.13). Note that the surface roughness is very important since it can directly affect the resistance measurement (Schroder, 2006). Therefore we need both steps of grinding, coarse grinding and fine grinding. After grinding, we dry the sample with nitrogen gas and should measure workpieces immediately to avoid the oxide occurring. The profile should be measured up to 150 data points

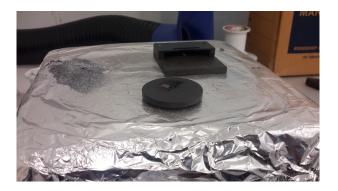


Figure 4.12 SRP sample mount on bevel block by melted wax.

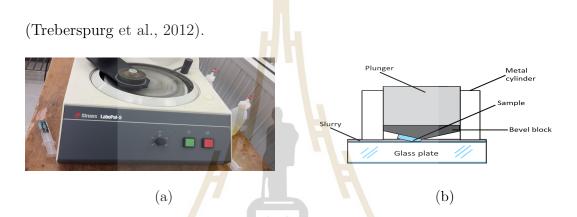


Figure 4.13 Polished with commercial wheels containing diamonds plate of different grain size (a) polishing machine at TMEC and (b) schematic of polishing sample for SRP measurement.

The measurement station consists of a movable xyz table, which is able to move in the minimal step of 1  $\mu$ m and carries two positioners holding probe tips. Successful measurements require a tungsten carbide probe of high hardness in order to penetrate the laver of silicon oxide and reduce the contact resistance (Dragicevic et al., 2013). For the following measurement tungsten carbide probes with a radius of 2  $\mu$ m have been used. For each measurement point, the table lowers down in step of 1 $\mu$ m every 500 ms.

#### Scanning Electron Microscope (SEM)

SEM images will be used to comparing with SRP results to confirm the epitaxial

layer thickness of silicon wafers. It also can verify the precision of the sample preparation and measurement in the SRP technique. More details about SEM results are given in appendix A.

#### C-V, I-V Measurement

The C-V method can provide the effective doping concentration Neff of semiconductor device, which would also include some information about active defects, and will be used in comparison with the dopant concentration from the SRP measurement (Dragicevic et al., 2013). Beside, both techniques I-V method allow us to get the resistance and leakage current which lead to the understanding of electrical properties and defect in the bulk of silicon.

### 4.3.2 Crystallographic Structure and Defect

Crystallographic structures of silicon wafers must be determined on the developing process in semiconductor technology. These include crystallographic orientation, size of the crystal grains in silicon, identification of crystalline phases and the characterization of the crystalline defects, such as dislocation, stacking faults, and precipitates. So we will use X-ray Diffraction (XRD) for determining substrate orientation, identifying crystalline phases and preferred orientations in polycrystalline layers and also structure of silicons wafer for identification of their chemical compositions. And AFM is used to determine the surface roughness of samples before and after irradiation. Both XRD and AFM results are given in appendix B.

### 4.3.3 Radiation sources

Gamma and electron irradiation are performed at the Thailand Institute of Nuclear Technology (Public Organization) (TINT). TINT provides radiation sources to bombard epi-HR silicon, Si-SiO<sub>2</sub> wafers and TEG diodes with different doses. The energy of the electron beam at TINT can be varied between 8-21.5 MeV but in this work, we use 10 MeV electron and gamma-ray source of 5 kGy/hr. Then, we compare damages of wafers caused by different particles at different radiation doses. For this research, in order to comply with the ALICE requirement, wafers should be able to tolerate at least 2700 Krad (TID) and 1.7x10e<sup>-12</sup> 1MeV.neq/cm<sup>2</sup> for NIEL.



### CHAPTER V

# EFFECT OF IRRADIATION ON SILICON DIODES

The studies of the properties changing in two different geometry CMOS diodes before and after irradiation of electron and gamma irradiation were done and shown in this chapter. For the radiation damage on CMOS diodes can be observed by electrical properties I-V and C-V characterization. Furthermore, by looking at the *N*eff and damage coefficient, it helps to determine the damage after irradiation of silicon diodes.

### 5.1 Studying of irradiation effect on CMOS Diodes

From the XRD results, we conclude that the changes in the SiO<sub>2</sub> part of the sensor are the main contribution to the degradation of the sensor. To investigate further, we creat two CMOS diodes of the same area of PN junctions but the difference in the area of SiO<sub>2</sub>. However, both of these diodes have been fabricated on a standard wafer, not the ALICE wafer, since we focus on the effects of the SiO<sub>2</sub> only. To study the radiation damage effect on electrical properties, we create the simplest semiconductor detector as a reverse-biased diode. Perimeter diode and area diode ( $D_A$  and  $D_P$ ) were designed with different perimeters to possess the different quantity of SiO<sub>2</sub>. But they are able to collect equivalent radiation dose rates. The schematic of both diodes are shown in figure 5.1. Then both diodes were radiated with 10 MeV electron at dose rate 20, 40, 60, 80 and 100 kGy. Besides

that diodes were radiated with <sup>60</sup>Co Gamma-ray at dose rate 100, 150, 200, 250, 300 kGy. We used all of the radiation sources at TINT. Radiation damage in diodes before and after were investigated by using I-V and C-V characterization at TMEC.

### 5.2 Diodes geometry and properties before irradiation

Diodes ( $D_A$  and  $D_P$ ) were designed with different perimeters to contain different quantities of SiO<sub>2</sub>.  $D_P$  comes with 40,400  $\mu$ m perimeters and 200 corners (figure 5.1(b)). For a  $D_A$ , its perimeter is 1,200  $\mu$ m with only 4 corners figure 5.1(a). Figure 5.1 shows the geometry of diode  $D_A$  and  $D_P$ . Both pictures are taken by a light microscope. Firstly, both of  $D_P$  and  $D_A$  are having the same area of 80,000  $\mu$ m<sup>2</sup>. For better understanding of diodes geometry, we show their schematic diagrams with dimensions in figure 5.2 and table 5.1. Both of diodes were characterized before irradiation by I-V, C-V characteristics as described in chapter IV .

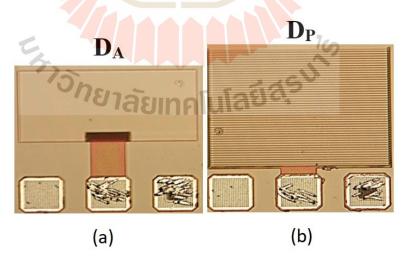
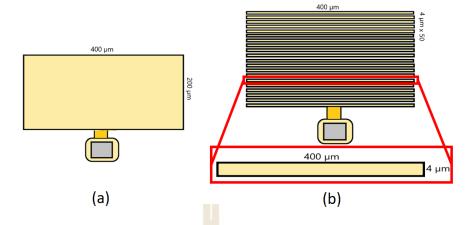
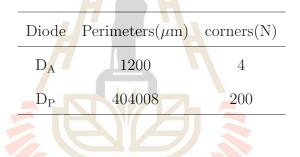


Figure 5.1 Images of  $D_A$  and  $D_P$  diodes from the microscope. Both diodes with area 80,000  $\mu$ m<sup>2</sup> difference perimeters were created. (a)  $D_A$  diode with 1,200  $\mu$ m perimeters, 4 corners, (b)  $D_P$  diode with 40,400  $\mu$ m perimeters, 200 corners.



**Figure 5.2** Schematic of  $D_A(left)$  and  $D_P(right)$  diodes.

Table 5.1 Geometry of  $D_A$  and  $D_P$  diodes.



Before irradiation the leakage current and capacitance of both diodes in figure 5.3(a) show that the leakage current of  $D_P$  (8.1 pA) is higher than that of  $D_A$  (1.4 pA) which demonstrates effect from the number of perimeters of diodes. Since the perimeter of the  $D_P$  is greater than  $D_A$ , so the perimeter current ( $J_P$ ) of  $D_P$  is higher than that of  $D_A$ .  $D_P(33.2 \text{ pF})$  capacitance from C-V characteristic before irradiation, is higher than that of  $D_A$  (22.2 pA) as a result from the number of perimeters of diodes (figure 5.3(b)).

The difference in leakage current comes from the combination of the area current scaling with diode area  $(J_A)$ , the perimeter current scaling with the perimeter  $(J_P)$  and the corner current scaling with the number of corners  $(J_C)$  (Czerwinski et al., 2003). Since the perimeter of the D<sub>P</sub> is greater than D<sub>A</sub>, so the perimeter

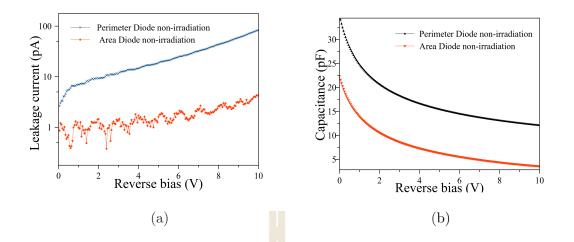


Figure 5.3 Leakage current (a) and Capacitance (b) of  $D_P$  and  $D_A$ , before irradiation.

current  $(J_P)$  of  $D_P$  is higher than that of  $D_A$ .

# 5.3 Current-Voltage characterization before and after irradiation

After electron irradiation, the leakage current of  $D_P$  and  $D_A$  were reported in figure 5.4(a) and figure 5.4(b) respectively. While after gamma irradiation, the leakage current of  $D_P$  and  $D_A$  were reported in figure 5.4(c) and figure 5.4(d) respectively. As a result, we observed an increase of leakage current with an increase in both electron and gamma radiation dose. It is expected that both ionization and displacement damage result in higher leakage current in the p-n junction.

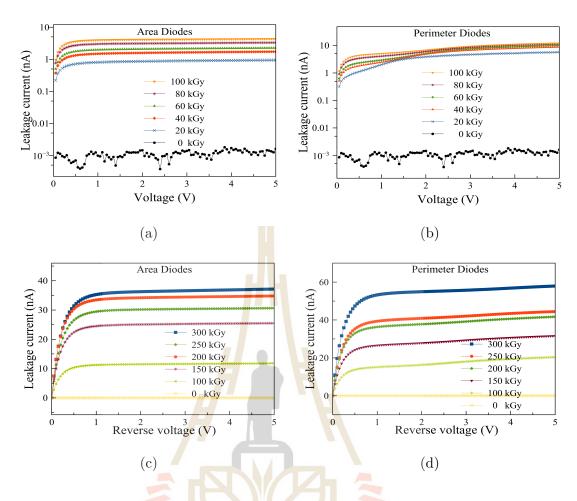


Figure 5.4 Leakage current of  $D_P$  and  $D_A$ , before and after irradiation (a)  $D_A$  on electron, (b)  $D_P$  on electron, (c)  $D_A$  on gamma and, (d)  $D_P$  on gamma, with different adsorption doses.

Then we have observed another interesting point about the amount of leakage current of  $D_P$  is much higher than that of  $D_A$ , in figure 5.4. For example in the case of the electron irradiation dose at 20 kGy, the leakage current of  $D_P$  is 3000 pA whereas the leakage current of  $D_A$  is 802 pA. Furthermore, it is indicated that the leakage current from gamma irradiation is higher than that of electron irradiation as shown in figure 5.4. The summary values of the leakage current for before and after irradiation of both diodes are obtained by fitting the I/V curve, as shown in figure 5.5(a).

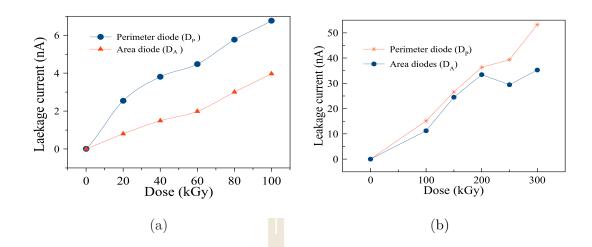


Figure 5.5 Fitting values of leakage current of (a) on electron, (b) on gamma.

# 5.4 Capacitance-Voltage characterization before and after irradiation

The capacitance of  $D_A$  and  $D_P$  before and after irradiation were reported in figure 5.6 and figure 5.7 respectively. C-V characteristics show a decrease in capacitance when the electron radiation dose increase as reported in figure 5.6. For example after the electron irradiation at the dose of 20 kGy, the capacitance of  $D_A$  and  $D_P$  decrease to 6.26 pF and 15 pF respectively as shown in figure 5.6(b) and figure 5.6(d). The results indicate that the number of perimeters contributes directly to the changes in capacitance after electron irradiation.

Figure 5.7 shows the C-V characteristics of  $D_P$  and  $D_A$  before and after gamma irradiation. The C-V curves show the capacitance of  $D_P$  lower than  $D_A$ that demonstrate effect of the number of perimeters to diodes. For reverse bias in C-V characterization the depletion region width (W) increases. W continues to increase further until it equates to the device thickness (d). The concept of depletion region width has been described in equation 4.9. Furthermore, while reverse bias, the potential barrier also rises to reduce the flow of majority carriers.

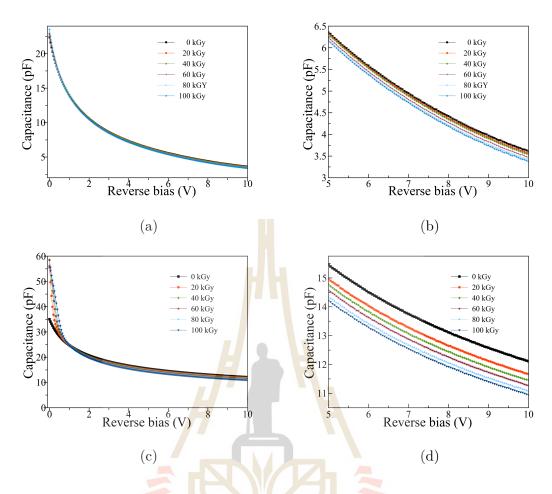


Figure 5.6 Capacitance of  $D_P$  and  $D_A$ , before and after electron irradiation (a)  $D_A$  on electron, (b) enlarger interval of  $D_A$  between 5-10 V on electron, (c)  $D_P$  on electron and (d) enlarger interval of  $D_P$  between 5-10 V on electron, with different adsorption doses.

From figure 5.6 and figure 5.7, it is observed that capacitances of both  $D_A$  and  $D_P$  diodes decrease with irradiation dose at high reverse bias (>1 in case of electron and >2 in case of gamma), whereas they increase at low reverse bias as shown in figure 5.8. The decrease in capacitance occurs because the injected carriers rapidly recombine with the built-in charge near the contact to produce a negative capacitance (dQ/dV) contribution. Occurring of carrier injection from the ohmic behavior depends on the maximum resistivity when we start applying

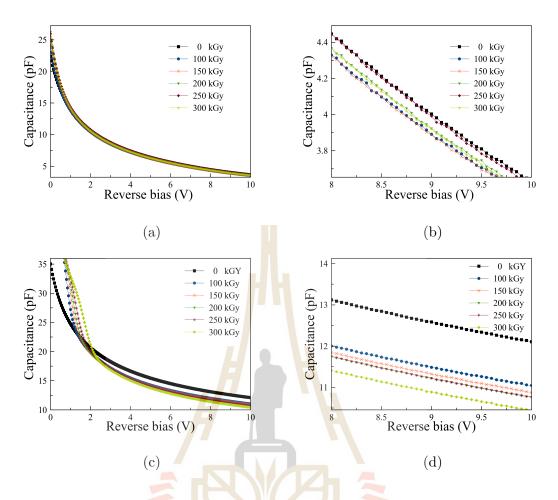


Figure 5.7 Capacitance of  $D_P$  and  $D_A$ , before and after gamma irradiation (a)  $D_A$  on gamma, (b) enlarger interval of  $D_A$  between 8-10 V on gamma, (c)  $D_P$  on gamma and (d) enlarger interval of  $D_P$  between 8-10 V on gamma, with different adsorption doses.

a voltage which is a dynamic property (McPherson, 2002). The study to assume the electrostatics of this effect was done in (Jones et al., 1998).

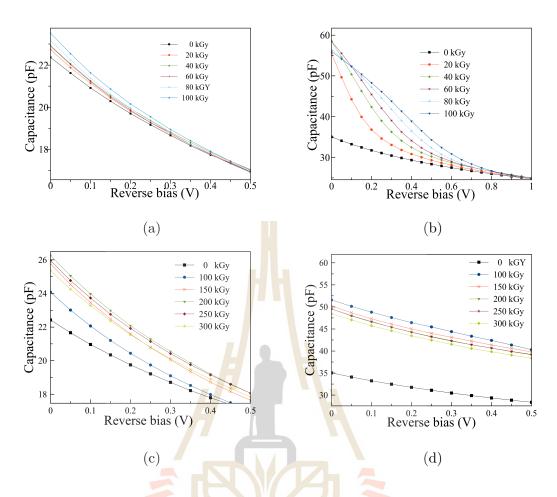


Figure 5.8 Capacitance at low reverse bias of  $D_P$  and  $D_A$  before electron and after gamma irradiation (a)  $D_A$  on electron, (b)  $D_P$  on electron, (c)  $D_A$  on gamma and (d)  $D_P$  on gamma, with different adsorption doses.

Figure 5.9, shows that capacitances of  $D_P$  and  $D_A$  at bias of 5 and 8 V slightly reduce with increasing radiation dose. This indicates that gamma irradiation can reduce capacitance of both  $D_P$  and  $D_A$  more than electron irradiation. But it is not clear at this stage which irradiation induces damage more than each other. In section 5.5 damage coefficient will be used to define irradiation damage to the capacitance.

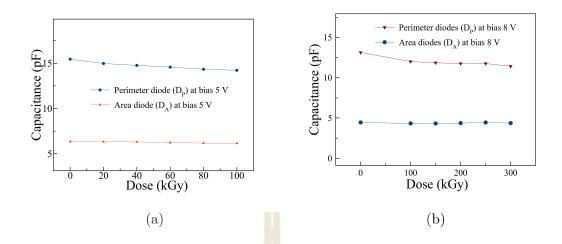


Figure 5.9 Fitting values of capacitance of  $D_A$  and  $D_P$  (a) electron and (b) gamma

### 5.4.1 Neff before and after irradiation

From C-V characterization, we can determine the effective doping concentration (Neff) by equation 4.3 which can be a parameter of radiation damage. The results of electron and gamma irradiation show the insignificantly change of Neff compared with the result measured before irradiated. By plotting the Neff versus the depletion width given by equation 4.9, the Neff below the junction can be found. Neff at each electron and gamma irradiation dose versus depletion width is shown in figure 5.10 and 5.11, respectively. After electron irradiation Neff of  $D_A$  and  $D_P$  reduce with irradiation dose as report in figure 5.10(a) and 5.10(c), respectively. It is easier to understand by looking at the figure 5.10(b) which is the enlarger version of  $D_A$  between 100-150  $\mu$ m and figure 5.11(c) which is the enlarger version of  $D_P$  between 45-65  $\mu$ m.

This indicates that electron and gamma irradiations have created a vary small impact on defects in CMOS diodes. Neff of  $D_A$  after gamma irradiation indicates that slightly change in Neff in high depletion width as shown in figure 5.11(a) and 5.11(b). For  $D_P$  the Neff obviously changes at lower depth as seen in figure 5.10 and 5.11.

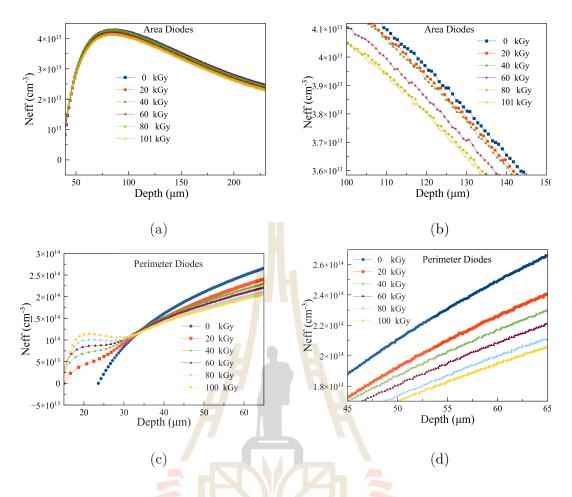


Figure 5.10 Neff of  $D_P$  and  $D_A$ , before and after electron irradiation (a)  $D_A$  on electron, (b) enlarger interval of  $D_A$  between 100-150  $\mu$ m on electron, (c)  $D_P$  on electron and, (d) enlarger interval of  $D_P$  between 45-65  $\mu$ m on electron, with different adsorption doses.

### 5.5 Damage coefficients

The impact of irradiation damage on leakage current can be described by a current damage coefficient  $(K_I)$ . The relation of the leakage current before  $(I_{R0})$  and after  $(I_{R\phi})$  on the damaging particle fluence, given by(Moritz et al., 2018)

$$I_{R\phi} = I_{R0} + K_I \phi. \tag{5.1}$$

Therefore,  $K_I$  at each of  $\phi$  is

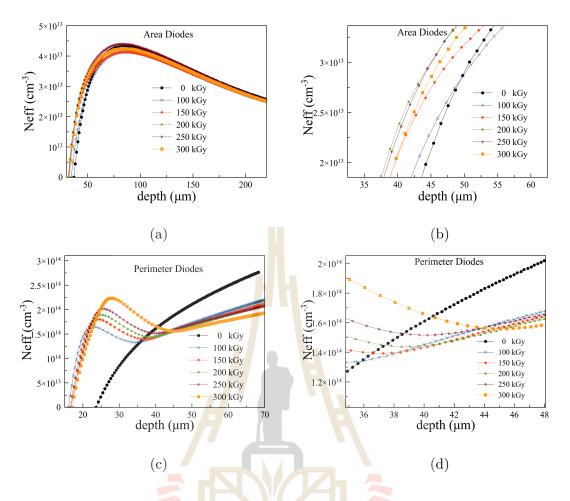


Figure 5.11 Neff of  $D_P$  and  $D_A$ , before and after gamma irradiation (a)  $D_A$  on gamma, (b) enlarger interval of  $D_A$  between 34-65  $\mu$ m on gamma, (c)  $D_P$  on gamma and (d) enlarger interval of  $D_P$  between 35-48  $\mu$ m on gamma, with different adsorption doses.

$$K_I = \frac{\partial I_R}{\partial \phi} \approx \frac{I_{R\phi} - I_{R0}}{\phi}.$$
(5.2)

From the current damage coefficient  $(K_I)$  shown in figure 5.12, it can be seen that electron irradiation creates non-linear effect in silicon diodes when reverse bias increases. But for gamma irradiations, the current damage coefficients change rapidly at reverse bias below 1 V.

After irradiation, an increase in resistivity is mostly observed which means

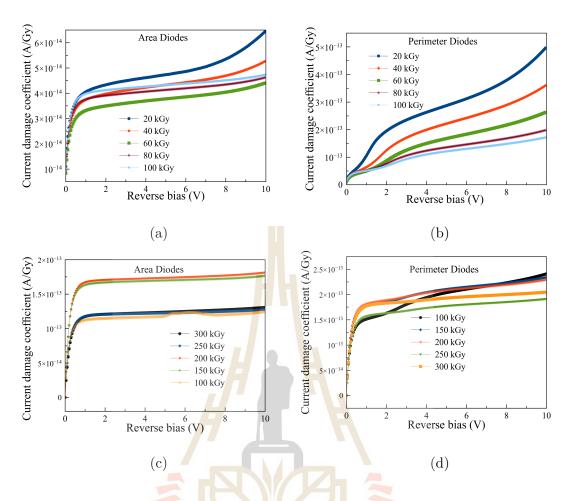


Figure 5.12 Current damage coefficient  $(K_I)$ , (a)  $D_A$  after electron irradiation, (b)  $D_P$  after electron irradiation, (c)  $D_A$  after gamma irradiation and, (d)  $D_P$  after gamma irradiation with different adsorption dose.

the increase of doping concentration. It results from the removal or reduction of free carriers occurring due to either the direct removal of dopants from active (substitutional) lattice sites by interaction with the created vacancies and interstitials which has been described in chapter III. These effects give rise to point defect complexes or the formation of dopants in a lattice site (interstitial) (Yamaguchi et al., 1996). To determine these effects the boron concentration is the one parameter that one can consider. The correlation between the boron concentration before  $[B_0]$  and after  $[B_{\phi}]$  irradiation is defined by (Taylor et al., 1998)

$$[B_{\phi}] = [B_0] - R_c \phi, \tag{5.3}$$

where  $R_C$  is the boron removal rate and  $\phi$  is the radiation dose (Gy). But in case of  $D_A$  and  $D_P$ , we will use the Neff to replace boron. Therefore, we can obtain Neff removal rate (Reff) in the same way

$$[Neff_{\phi}] = [Neff_0] - Reff\phi.$$
(5.4)

By knowing the Neff at a certain depth below the junction before and after irradiation, Reff at each dose ( $\phi$ ) can be obtained from

$$Reff = \frac{\partial Neff}{\partial \phi} \approx \frac{[Neff_0] - [Neff_{\phi}]}{\phi}.$$
 (5.5)

Reff can be calculated from equation (5.5) and is shown in figure 5.13.

The starting point is the relation between [B] and C for a uniform doping profile, which is given by

$$[B] = \frac{2(V_R + V_{bi})}{A^2 q \epsilon_{Si}},\tag{5.6}$$

where  $V_R$  is the reverse bias,  $V_{bi}$  is the Built-in potential, A is area of the junction, q is the elementary charge (= 1.602x10<sup>-19</sup> C) and  $\epsilon_{Si}$  is the dielectric permittivity of silicon (=1.05315x10<sup>-12</sup> F/cm).

By replacing [B] from equation (5.6) in to equation (5.3), we can obtain the capacitance damage coefficient

$$C_{\phi}^2 = C_0^2 - K_C \phi, \tag{5.7}$$

$$K_C = \frac{\partial C}{\partial \phi} \approx \frac{C_0^2 - C_\phi^2}{\phi},\tag{5.8}$$

where  $C_0, C_{\phi}$  and  $K_C$  are the capacitance before, after irradiation and the capac-

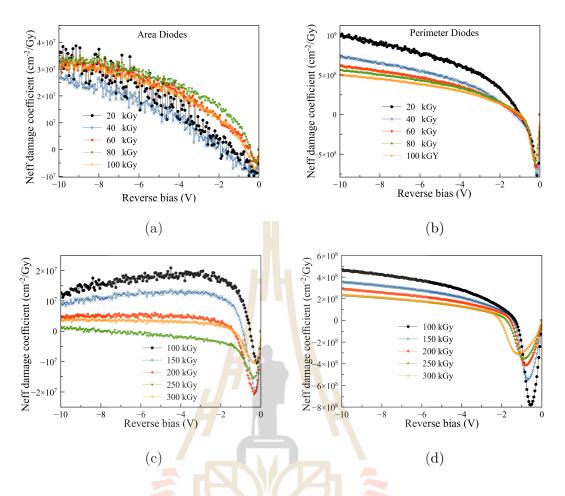


Figure 5.13 Neff damage coefficient  $(K_C)$  versus reverse bias, (a)  $D_A$  after electron irradiation, (b)  $D_P$  after electron irradiation, (c)  $D_A$  after gamma irradiation and, (d)  $D_P$  after gamma irradiation with different adsorption dose.

itance damage coefficient respectively. Figure 5.14(a) and 5.14(b) show  $K_C$  after electron irradiation of  $D_A$  and  $D_P$ , respectively, figure 5.14(c) and 5.14(d) show  $K_C$  after gamma irradiation of  $D_A$  and  $D_P$ , respectively.

From figure 5.14 it is observed that  $K_C$  of  $D_P$  higher than that of  $D_A$ . And all of the results show that the changing of electronic properties does not depend linearly on irradiation. This can only conclude that the electron irradiation has a higher effect on both diodes than gamma irradiation, and also a higher effect on  $D_P$  than  $D_A$ . Therefore, the irradiation effect has a higher effect on the

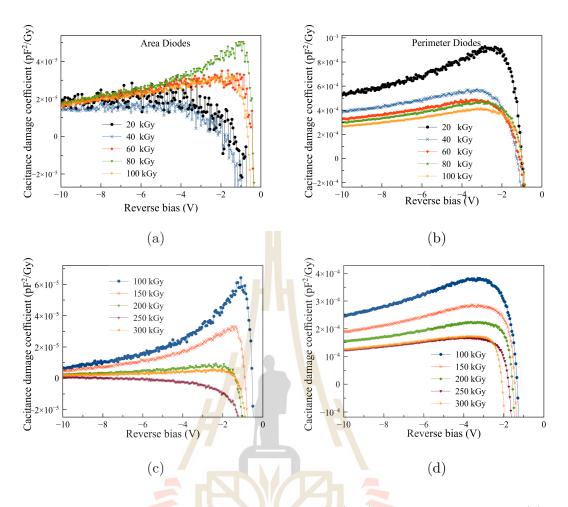


Figure 5.14 Capacitance damage coefficient  $(K_C)$  versus reverse bias, (a)  $D_A$  after electron irradiation, (b)  $D_P$  after electron irradiation, (c)  $D_A$  after gamma irradiation and, (d)  $D_P$  after gamma irradiation with different adsorption dose.

peripheral capacitance than on the area capacitance. For gamma irradiation, C is not proportional to  $\phi$ , and the highest  $K_C$  is found at the low dose. In figure 5.14, we can see the significantly changing of  $K_C$ , at a low radiation dose than that of at the radiation high dose, which indicates that at a low radiation dose, diodes change their properties more than at a high radiation dose.

### 5.6 Summary

I-V characteristics show the increase in leakage current linearly after irradiation as shown in figure 5.5. Conversely, C-V characteristics show the decrease in capacitance linearly after irradiation as shown in figure 5.9. As expected, the shape and size of the diode perimeter which is related to geometry and pattern of a circuit on the sensor contribute directly to the changes in electrical properties after irradiation.

The experimental results after irradiation show that the leakage current for both  $D_A$  and  $D_P$  increases due to the increase of irradiation dose as shown in figure 5.5. Conversely, the capacitance of both diodes decreases while the irradiation dose is increased as shown in figure 5.9. As expected, after irradiation, the leakage current of  $D_P$  is higher than  $D_A$  since  $D_P$  contains a higher amount SiO<sub>2</sub> more than that of  $D_A$ . But for the capacitance of  $D_A$  after irradiation is higher than that of  $D_P$ . These results have confirmed that the quantity of silicon dioxide in the electronic devices is the main contribution to the device damages after irradiation.

The irradiation effect has a higher effect on the peripheral capacitance than on the area capacitance. The results indicate that the number of perimeters contributes directly to the changes in electrical properties after irradiation.

# CHAPTER VI CONCLUSION

The effect of 10 MeV electron and gamma irradiation at different dose, on the structural and electrical properties of two different geometry of CMOS diodes have been studied. I-V characteristics show the increase in leakage current after irradiation. Conversely, C-V characteristics show the decrease in capacitance linearly after irradiation. As expected, the shape and size of the diode perimeter which is related to geometry and pattern of a circuit on the sensor contribute directly to the changes in electrical properties after irradiation.

We conclude that the changes in the SiO2 part of the sensor are the main contribution to the degradation of the sensor. Subsequently, the experimental results after irradiation show that the leakage current of  $D_P$  is higher than  $D_A$ since  $D_P$  contains a higher amount of SiO<sub>2</sub> more than that of  $D_A$ . But for the capacitance of  $D_A$ , after irradiation, is higher than that of  $D_P$ . These results have confirmed that the quantity of silicon dioxide in the electronic devices is the main contribution to the device damages after irradiation. From looking at damage coefficient ( $K_I$ ,  $K_C$  and Reff), it indicates that the electrical properties do not depend linearly on irradiation dose, since the material have the limitation for structural changes.

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## APPENDICES



### APPENDIX A

### ALICE WAFER CHARACTERIZATION

We investigate the high resistivity silicon wafer from ALICE of 25  $\mu$ m epilayer thickness using Spreading Resistance Profiling (SRP) measurement to measure its resistivity, dopant concentration, and epitaxial layer depth. Then we use the Scanning Electron Microscope (SEM) to verify results by looking at its cross-section physically. For the physical wafer characterization the four-point probes technique is applied to the wafer.

#### Epitaxial thickness of ALICE silicon wafer properties

Suranaree University of Technology (SUT) has collaborated with Thai Micro Electronic Center (TMEC), and A Large Ion Collider Experiment (ALICE) to develop a new silicon sensor for the Inner Tracking System (ITS) for particle tracking in high energy physics. In this project, the ALICE new sensor is requested to be 50 microns thick, the reason is to reduce its material budget that relate directly with the thickness of the sensor. Consequently, ALICE proposes to use ultrathin silicon wafers with 25 microns thickness and high resistivity. First, wafers are measured the doping concentration and epitaxial layer depth by using Spreading Resistance Profiling (SRP) and Scanning Electron Microscope (SEM). After wafer characterization, our results show that it is possible to obtain a high resistivity wafers up to 1.6 k $\Omega$ ·cm with an epitaxial layer of 25 microns to be starting materials for ALICE PIxel DEtector (ALPIDE) sensor.

At the beginning to confirm and characterize the epitaxial layer thickness

and resistance geometry of high resistivity silicon wafer from ALICE, the wafer was investigated by looking at geometric and electrical properties using several techniques and measurement. The surface resistivity is performed by using the 4PP method to modeling the resistance topology of the whole surface of a silicon wafer, as shown in figure A.1.

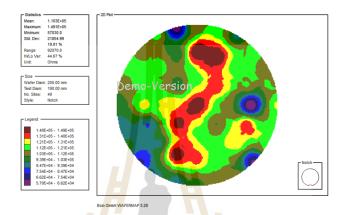


Figure A.1 Sheet resistance of high resistivity silicon wafer.

To define the epitaxial layer thickness we use the SRP measurement technique. In the measurement, samples have been cut in size  $3x1 \text{ cm}^2$ . Each sample comes from five different zones of the silicon wafer composite top, bottom, left, right and center. Then we mount it with melted wax on the bevel block 1° (figure 2). Next, we polish the sample with a polishing wheel which contains with diamond polishing compound size 1  $\mu$ m for coarse grinding and size 0.25  $\mu$ m for fine grinding. Note that the surface roughness is very important since it can directly affect the resistance measurement. Therefore we need both step of grinding, the coarse grinding and the fine grinding. After grinding, we dry the sample with nitrogen gas and measure workpieces immediately to avoid the oxide occurrence.

The measurement is done by using tungsten carbide probes of high hardness to penetrate the natural silicon oxide and reduce the contact resistance. The result shows resistivity as a function of depth. It is determined by applying a voltage

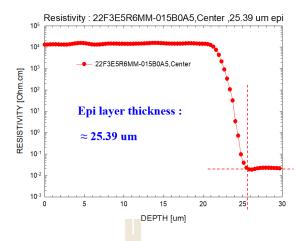


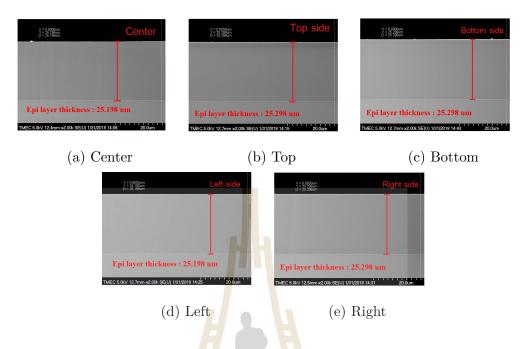
Figure A.2 Resistivity profiling measured at different depths in the silicon wafer. ramp across the probes where the measured resistance is dominated by spreading resistance effect as shown in figure A.2.

In next step, the SEM is used for imaging the thickness of the whole silicon wafer, in figure A.3 shown that the wafer thickness is 748 µm. After that, SEM is used to define the epitaxial layer that has been growing on this wafer and also can take the result to confirm the accuracy of the SRP technique that is shown in figure A.2.



**Figure A.3** SEM cross-sectional show the thickness of high resistivity silicon wafer.

Samples from five different areas on a silicon wafer was selected from the



center, top, bottom, left and right side, as shown in the figure A.5.

Figure A.4 SEM cross section to define epitaxial layer thickness of five different areas in the silicon wafer are shown in (a) 25.198  $\mu$ m from the top, (b) 25.298  $\mu$ m from the bottom, (c) 25.298  $\mu$ m from the left, (d) 25.298  $\mu$ m from the right and (e) 25.198  $\mu$ m from the center.

From the SEM results are shown in figure A.4, we can verify the epitaxial layer thickness by looking at its cross-section physically from five different areas in the silicon wafer. The results of epitaxial layer thickness are given in table A.1.



Figure A.5 Selection of samples from silicon wafer.

Picture	Epitaxial thickness ( $\mu m$ )
(a) Top	25.198
(b) Bottom	25.298
(c) Left	25.298
(d) Right	25.298
(e) Center	25.198
Average	25.258

Table A.1 The results of five different areas of the silicon wafer.

Table A.1 indicates that the epitaxial layer thickness of high resistivity silicon wafer from ALICE is 25  $\mu$ m in the whole of wafer evenly.

#### Summary and conclusions

We have shown that the corresponds Epitaxial layer thickness for the SRP technique and SEM give a similar distance around 25.3  $\mu$ m. Hereby it implies that the sample preparation was acceptable with precision. In the part of resistivity measurement with SRP, we get the resistivities above 1 k $\Omega$ ·cm from the depth in the range of 0-20  $\mu$ m. Then the resistivity reduces sharply between 21-25  $\mu$ m. Thus, the result indicates that the thin silicon wafer poses the resistivity more than 1 k $\Omega$ ·cm which sufficient to be used as a starting material for the new sensor construction for ALICE ITS upgrade.

### APPENDIX B

# RADIATION DAMAGE ON ALICE AND SiO<sub>2</sub> WAFER

In this appendix, the effects of electron and gamma irradiation on a high resistivity silicon wafer and  $Si-SiO_2$  silicon wafer were considered. Gamma and electron at different radiation doses were radiated at the wafer to study the crystal and surface damages from irradiation. Then both wafers were studied by material characterization techniques, X-Ray Diffraction (XRD) and Atomic Force Microscope (AFM) before and after irradiation.

#### Irradiation on epi-HR silicon wafer

All samples were irradiated with gamma and electron source at room temperature in an ambient atmosphere, with the energy of 10 MeV or 10 kGy/s for electron and 5 kGy/hr for gamma source at TINT. The microstructure and chemical composition analysis unirradiated and irradiated samples of the high resistivity silicon wafer were performed using XRD. Then, the surface of high resistivity Si before and after irradiation was investigated using AFM. The adsorption dose rate D = 5 kGy/hr at the different adsorbed dose of 0, 100, 150, 200, 250, 300 kGy for gamma source were selected. Adsorption dose rate D = 10 kGy/s at the different adsorbed dose of 0, 20, 60, 80, 100 kGy for electron source were also chosen. The microstructure analysis of unirradiated and irradiated Si/SiO<sub>2</sub> samples and high resistivity silicon wafer were performed using D8 ADVANCE X-ray diffractometer (XRD) with Cu K $\alpha$  radiation ( $\lambda = 1.540598 \text{ Å}$ ).

#### XRD results of irradiated epi-HR silicon wafer

The X-ray diffraction patterns obtained from high resistivity silicon wafer both before and after 10 kGy/s of electron and 5 kGy/hr of gamma irradiation affected with different adsorption dose are shown in figure B.1. The XRD patterns of high resistivity silicon wafers before and after gamma irradiation effect with adsorption dose of 0, 100, 150, 200, 250 and 300 kGy, are shown in figure B.1(a)and B.1(b). The pattern reflects the characteristic of before and after electron irradiation which could not affect though the crystal structure of high resistivity silicon wafer with 25  $\mu$ m epitaxial layer. This pattern demonstrated that all of the different adsorption doses are the amorphization of the epitaxial silicon wafer. At the same time, the high resistivity silicon wafer before and after electron irradiation effect with an adsorption doses rate of 0, 20, 40, 60, 80 and 100 kGy demonstrated that the patterns have not changed in the XRD patterns both before and after irradiation as seen in figure B.1(c) and B.1(d). The result demonstrated that in absorption dose range 0-100 kGy electron radiation could not affect the crystal structure change of high resistivity silicon wafer with 25  $\mu$ m epitaxial layer. It is interesting to point out that there is no distinct sharp peak at all. This implies the amorphization properties of the epitaxial layer.

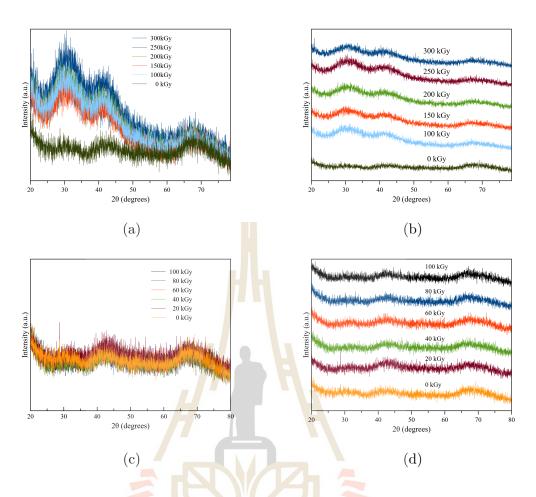
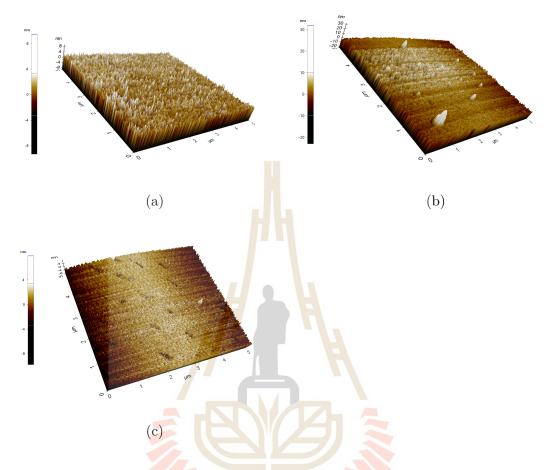


Figure B.1 XRD pattern of high resistivity silicon wafer both before and after (a-b) electron and (c-d) gamma irradiation effect with different adsorption dose rate.

### AFM results of irradiated epi-HR silicon wafer

The surface morphology of epi-HR silicon wafer before and after high-energy electron and gamma irradiation by AFM are shown in figure B.5. AFM images of the non-irradiation epi-HR silicon wafer are represented in figure B.2(a). It can be observed that there are rugged in the silicon matrix. While after gamma irradiation, our observation shows the precipitations exist in the silicon matrix (figure B.2). In contrast, after electron irradiation, it generates radiation defects like hole in the entire silicon structure comparing to that of before irradiation as shown in figure B.2(c).



**Figure B.2** Surface morphology of epi-HR silicon wafer, (a) non-irradiation , (b) gamma irradiation at 300 kGy and (c) electron irradiation at 100 kGy.



## Irradiation on $SiO_2$ silicon wafer

The microstructure analysis unirradiated and irradiated samples of Si/SiO<sub>2</sub> and high resistivity silicon wafer were performed using a D8 ADVANCE X-ray diffractometer (XRD) with Cu K $\alpha$  radiation ( $\lambda = 1.540598$  A).

### XRD results of irradiated $SiO_2$ silicon wafer

The XRD patterns of Si-SiO<sub>2</sub> wafer both before and after the electron (10 kGy/s) and gamma (5 kGy/hr) irradiation with difference adsorption dose of 0,

100, 150, 200, 250 and 300 kGy for gamma irradiation and 0, 20, 40, 60, 80 and 100 kGy for electron irradiation are shown in figure B.3(b). The Si-SiO<sub>2</sub> wafer both before and after the gamma irradiation with difference adsorption dose of 0, 100, 150, 200, 250 and 300 kGy are shown in figure B.3(a), XRD patterns of all samples show sharp diffraction peaks at  $2\theta = 33$ , 56.3 and 61.8°. Among them, the diffraction peaks at 33 and  $61.8^{\circ}$  are the strongest. The sharp diffraction peaks at  $2\theta = 33^{\circ}$  (figure B.4(a)) of the Si-200 reflection of Si(100) substrate (Zaumseil, 2015) and 56.3° (figure B.4(c)) also related to Si(100) substrate (Dai et al., 2018) and another sharp diffraction peaks at  $2\theta = 61.8^{\circ}$  (figure B.3(e)) related to the crystallization of  $SiO_2$ . The XRD pattern of non-irradiation, 100, 150 and 200 kGy showed two main structures of Si(100) substrate and  $SiO_2$ . An increase in the gamma irradiation to 250 - 300 kGy, the peaks of Si(100) disappear, while crystalline peaks of  $SiO_2$  as indicated by the typical peak at 61.8° decreases with the increasing of gamma irradiation. Figure B.4(e) shows the magnification of 61.8° peaks where peaks shift to lower  $2\theta$  values as the irradiation increases, suggesting larger lattice parameters or crystal structure.



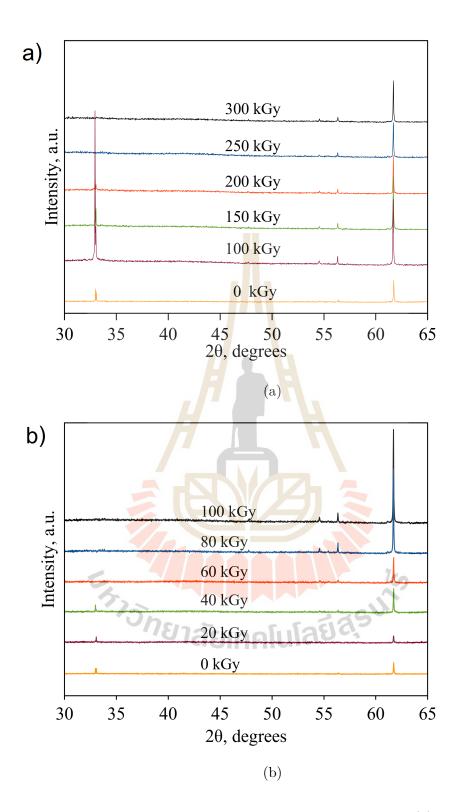


Figure B.3 XRD pattern Si-SiO<sub>2</sub> wafer, before and after (a) gamma and (b) electron irradiation with different adsorption dose of 100, 150, 200, 250, 300 kGy and 20, 40, 60, 80, 100 kGy, repressively.

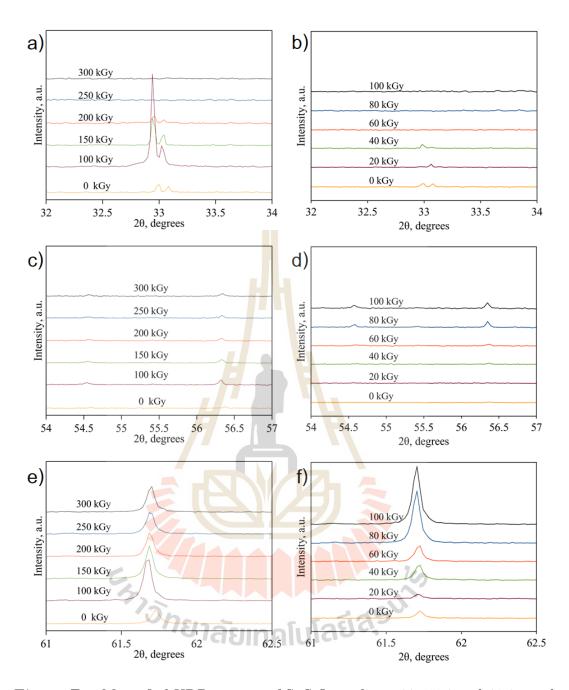
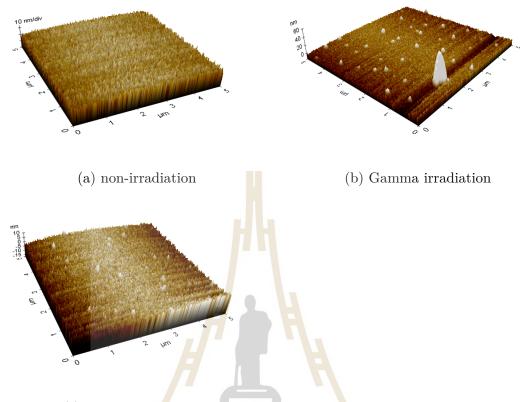


Figure B.4 Magnified XRD spectra of  $Si-SiO_2$  wafer at 33, 55.6 and 61.8° peaks, before and after irradiation with different adsorption dose which a, c, e for gamma and b, d, f for electron.

At the same time, the  $Si-SiO_2$  wafer both before and after the electron irradiation with difference adsorption dose of 0, 20, 40, 60, 80 and 100 kGy are shown in figure B.3(b). The XRD patterns of all samples show sharp diffraction peaks at  $2\theta = 33^{\circ}$  (figure B.4(b)) of the Si-200 reflection of Si(100) substrate (Zaumseil, 2015) and another sharp diffraction peaks at  $2\theta = 61.8^{\circ}$  (figure B.4(f)) related to the crystallization of SiO<sub>2</sub>. The XRD pattern of non-irradiation, 20 and 40 kGy showed two main structures of Si(100) substrate and SiO<sub>2</sub>. These XRD results suggest that the sharp peaks of Si(100) are still  $2\theta = 33^{\circ}$  decreasing and  $2\theta = 61.8^{\circ}$  increasing, we note that the sharp peaks exhibited the long-range order of a crystal. An increase in the electron irradiation to 60 - 100 kGy, the peaks of Si(100) disappear but the peaks of Si(100) substrate still appeared (Dai et al., 2018). The crystalline peaks of SiO<sub>2</sub> as indicated by the typical peak at  $61.8^{\circ}$  increases with the increase of electron irradiation. Figure B.4(f) shows the magnification of  $61.8^{\circ}$  peaks where peaks shift to lower  $2\theta$  values as the irradiation increases, suggesting larger lattice parameters or crystal structure.

## AFM results of irradiated $SiO_2$ silicon wafer

The AFM surface morphology of Si-SiO<sub>2</sub> before and after high-energy electron irradiation are shown in figure B.5. AFM images of the non-irradiation wafer are represented in figure B.5(a), it can be observed the fine roughness in the SiO<sub>2</sub> matrix. While after gamma irradiation, AFM showed the precipitations exist in the SiO<sub>2</sub> matrix (figure B.2(b)). For electron irradiation, it generates radiation defects on the entire Si-SiO<sub>2</sub> structure when we compare to that of before irradiation as shown in figure B.5(c). It is in qualitative agreement with the data reported in (Kaschieva and Dmitriev, 2017). It is reported that the radiationenhanced diffusion of oxygen taking place which was observed in (Kaschieva et al., 2012; Kaschieva et al., 2010). Moreover this can be the reason for the creation of Si nanocrystals in the SiO<sub>2</sub> oxide of the implanted samples (Kaschieva and Dmitriev, 2017). But we cannot confirm that because we need more time to



(c) Electron irradiation

**Figure B.5** Surface morphology of  $Si-SiO_2$  wefer, (a) non-irradiation , (b) gamma irradiation at 300 kGy and (c) electron irradiation at 100 kGy.

investigate defects occuring in figure B.5(c) to see if they caused by oxygen or not. Kaschieva's work showed that the Si nanocrystals in SiO<sub>2</sub> of the implanted Si-SiO<sub>2</sub> structure was created only after MeV electron irradiation and the shape and density of Si nanocrystals depended on the type of implanted ions(Kaschieva et al., 2012; Kaschieva et al., 2010). In contrast to Kaschieva et al (Kaschieva et al., 2012; Kaschieva et al., 2010), our study indicates similar result at 300 kGy gamma irradiation as well (see figure B.5(b))

#### Summary and conclusions

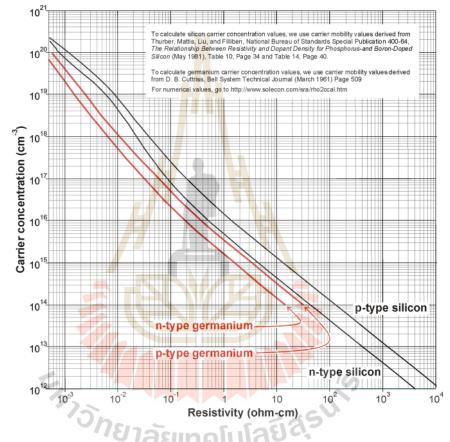
The effect of electron and gamma irradiation on the structural and surface morphology of ep-HR Si wafer and Si/SiO<sub>2</sub> wafer have been studied. The XRD patterns show the sharp diffraction peak of Si/SiO<sub>2</sub> and increase the crystallinity of SiO2 after irradiation. The shift of SiO<sub>2</sub> (61.8°) XRD peak to a smaller angle  $(2\theta)$  indicate that the crystalline sizes decrease linearly after irradiation which can be confirmed by Scherer's equation calculation. In contract to ep-HR Si wafer, our study indicates that there is no structural change if the irradiation dose from the electron beam is less than 100 kGy and gamma ray is less than 300 kGy.

From the XRD results, we conclude that the changes in the SiO<sub>2</sub> part of the sensor are the main contribution to the degradation of the sensor. To investigate further, we create two CMOS diodes of the same area of PN junctions but the difference in the area of SiO<sub>2</sub>. However, both of these diodes have been fabricated on a standard wafer, not the ALICE wafer, since we focus on the effects of the SiO<sub>2</sub> only. Perimeter diode ( $D_P$ ) and area diode ( $D_A$ ) were designed with different perimeters to possess the different quantity of SiO<sub>2</sub> but able to collect equivalent radiation dose rates the schematic of both diodes shown in figure 5.1.

The surface morphology of ep-HR Si and Si-SiO<sub>2</sub> wafer after both electron and gamma irradiation are shown in figure B.2 and B.5. It is important to note that the effect of electron and gamma irradiation affected to the wafer surface which requires further studies.

# APPENDIX C

# SILICON PROPERTIES



**Figure C.1** Diagram of the relationship between resistivity and impurity dopant concentration for silicon N-type and P-type (laboratories, 2010).

Structural and mechanical	
Group	IV
Atomic number	14
Atomic weight $(g \cdot mol^{-1})$	28.0855
Atoms, total $(cm^3)$	$4.995 \times 10^{22}$
Crystal structure	Diamond (fcc)
Lattice constant( $\dot{A}$ )	5.43
Symmetry Group	$O_h^7$ -Fd3m
Oxidation state	-4, (+2), +4
Electron configuration	$1s^2 2s^2 2p^6 3s^2 3p^2$
Density (g/cm <sup>3</sup> )	2.33
Electronegativity according to Pauling	1.8
Isotopes	5
Band Gap Type	Indirect
Density of surface atoms $(cm^2)$	(100) $6.78 \times 10^{14}$
	(110) $9.59 \times 10^{14}$
E,	(111) $7.83 \times 10^{14}$
Young's modulus (GPa)	190 (111) crystal orientation 7
Yield strength (GPa)	7
Fracture strain	4%
Poisson ratio,	0.27
Knoop hardness $(kg/mm^2)$	850
Electrical	
Electrical Energy gap (eV)	1.12
Intrinsic carrier concentration $(cm^3)$	$1.38 \times 1010$
Intrinsic resistivity ( $\omega$ -cm)	$2.3 \times 105$

Dielectric constant $(\epsilon)$	11.8	
Mobility (drift) $(cm^2/V-s)$	$1500 \ (electrons)$	
	475  (holes)	
Temperature coeff. of resistivity (Ke	61) 0.0017	
Diffusion coefficient electrons	$\leq 36 \text{ cm}^2/\text{s}$	
Diffusion coefficient holes	$\leq 12 \text{ cm}^2/\text{s}$	
Electron thermal velocity	$2.3 \times 10^5 \mathrm{m/s}$	
Hole thermal velocity	$1.65 \times 10^5 \mathrm{m/s}$	
Thermal		
Coefficient of thermal expansion (°C	$(2^{1})$ 2.6 × 10 <sup>6</sup>	
Melting point (°C)	1414	
Boiling point(°C)	3265	
Specific heat (J/kg-K)	700	
Thermal conductivity (W/m-K)		
Thermal diffusivity	$0.8 \text{ cm}^2/\text{s}$	
Optical		
Index of refraction 3.42	$\lambda = 632 \text{ nm}$	
ບັນລັຍເກຄໂນໂລຍ $3.48 \lambda = 1550 \text{ nm}$		
Energy gap wavelength	1.1 $\mu {\rm m}$ (transparent at larger wavelengths)	
Absorption	$>106~{\rm cm^1}~\lambda=200360~{\rm nm}$	
	$10^5 \text{ cm}^1 \lambda = 420 \text{ nm}$	
	$10^4 \text{ cm1 } \lambda = 550 \text{ nm}$	
	$103 \text{ cm}^1 \lambda = 800 \text{ nm}$	
	$<0.01~{\rm cm^1}~\lambda=1550~{\rm nm}$	

The orientation of the surface crystal plane of a certain silicon wafer, as well as the doping type on wafers, are practically impossible to visually identify with distinct cuts called flat. A flat helps distinguishes between p-type and n-type wafers of different orientations are shown in figure C.2.

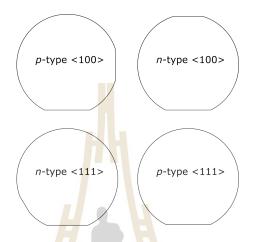


Figure C.2 Schematic illustration of the primary and secondary flats used for the identification of silicon wafers.



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### PUBLICATIONS

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